Migrating Spartan 6 Design to 7 Series & Beyond

WP03 – Hardware Design Considerations

Adiuvo Engineering

Abstract – Migration from an AMD-Xilinx Spartan®-6 device to a more modern 7 Series device requires not only device and tool chain migration but also the requirement to update the design of the circuit board. This white paper is intended to demonstrate the major differences and challenges in migrating from Spartan-6 to 7 series design at the hardware level.

To help designers make the transition, this white paper will address:

- Packaging differences
- Power architecture differences and sequencing
- Power Estimation
- IO Planning
- Clock Planning
- Memory changes

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Introduction

This white paper outlines the key changes which must be considered when updating an electronic circuit board design to migrate from a Spartan-6 FPGA (Field Programmable Gate Array) to a 7 series device or beyond. This white paper will look at selecting the most appropriate package, understanding the power architecture and sequencing.

Once the fundamentals of packing and power supply requirements have been understood, the white paper will further introduce power estimation, IO banking, pin planning, and how to design for high-speed DDR (Double Data Rate) memory interfaces.

Packaging Differences

One of the major differences between Spartan-6 FPGA and 7 series and UltraScale™ devices is in the packaging, pin out, and available IO. Spartan-6 devices offer the developer a range of packages from the Quad Flat Pack TQ144 package to the Fine Grid 900 Ball Grid Array. This range of devices provides the developer between 102 and 576 IOs which can be used.

7 series and UltraScale devices do not provide a package in quad flat pack package; however there are a range of other packages available which provides the developer with the IO density required.

The table below can be used to aid selection of the correct package which provides the necessary IO density.

Table 1 – IO Density Migration

S6 Package	S6 User IO	S7 Package	A7 Package	K7 Package	KUS Package
TQ144	102	CSGA225	CPG236	FBG484	NA
CPG196	106	CSGA225	CPG236	FBG484	NA
CSG225	160	CSGA324	CSG324	FBG484	NA
FFG256	186	CSGA324	FGG484	FBG484	NA
CSG324	232	FGGA484	FGG484	FBG676	NA
FGG484 / CSG484	338	FGGA484	FGG676	FBG676	NA
FG676	498	NA	FGG1156	FBG900	NA
FG900	576	NA	NA	NA	A1517

In addition to the IO density, the IO type must be selected appropriately. Spartan-6 devices offer a single IO Bank type which can implement IO standards from 3v3 to 1v2 single ended standards and differential standards such as LVDS (Low Voltage Differential Signalling).

7 series and UltraScale devices provide two different classes of IO bank - high performance and high range. High range banks provide voltage standards from 3v3 to 1v2 along with several differential standards including those commonly used for communication e.g., LVDS and those commonly used with DDR3 and DDR3L, such as DIFF_SSTL135 and DIFF_SSTL15.

Higher performance banks, provide the developer with higher performance IO Standards intended for use in high bandwidth chip-to-chip and memory interfaces. High performance IO banks support voltage standards up to 1v8 and provide additional features beyond that provided by High range banks such as Digitally Controlled Impedance and fine output delays.

Table 2 – IO Features

Feature	HP Bank	HR Bank
3.3v IO Standard	NA	Supported
2.5v IO Standard	NA	Supported
1.8v IO Standard	Supported	Supported
1.5v IO Standard	Supported	Supported
1.35v IO Standard	Supported	Supported
1.2v IO Standard	Supported	Supported
LVDS	Supported	Supported
VCCAux IO	Supported	NA
DCI	Supported	NA
Internal Vref	Supported	Supported
Diff Term	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	NA
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD Delay	NA	Supported

When selecting devices for IO migration, not only must IO density be considered, but the developer must also ensure the IO density is sufficient in each of the HP (High Performance) and HR (High Range) banks provided.

Power Architecture

The major difference between the Spartan-6 devices and 7-series devices is in the power architecture.

The main supplies for the Spartan-6 devices are the core, auxiliary, IO bank voltages, along with the battery and fuse supplies. Powering up or down a Spartan-6 device does not require any sequencing of the power rails.

7 series devices have similar power requirements with core, auxiliary, BRAM, IO bank voltages, battery, and ADC supplies. Just like with Spartan-6 power supplies, several supplies which use a common voltage can be supplied from the same regulator

Of course, as the 7 series devices are fabricated at a lower node (28nm) compared to Spartan-6 device's 45 nm, the core voltage is reduced. This lower node also means the overall power consumption is reduced and performance of the device is increased when compared to Spartan-6 devices.

In a change from the Spartan-6 solutions, there is a need for power supply sequencing on power up and down in 7 series devices. Developers should pay consideration to the 7 series AC and DC Switch characteristics data sheet. If a Zynq 7000 is to be used, then answer record AR 65240 must be followed to prevent impacts on the device EFUSE.

Failure to follow the power supply sequencing can result in increased currents being drawn during power on, or failure of the IO to enter a tri-state.

To address both the current and the sequencing requirements, designers often use a Power Management IC (PMIC) device. These devices are available in a range of capabilities to meet the FPGA power rail requirements while also enabling programmable rail sequencing. PMIC also often support in-circuit power management using PMBus over I2C, which enables power levels to be set and prognostics such as current draw etc. to be monitored in real time. One typical implementation from the Digilent Arty S70-50 can be seen below, where a single PMIC provides all the rails necessary.

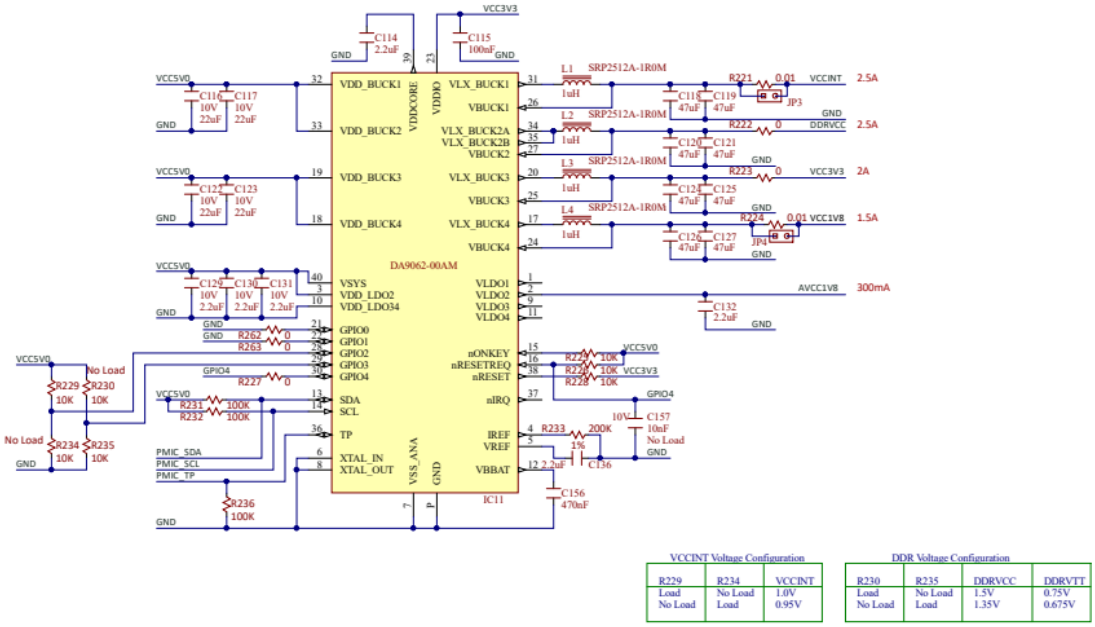

Figure 1 – Digilent Arty S7-50 Power Architecture (source Digilent)

Power Estimation

To correctly size the power architecture, we need an accurate estimation of the power requirements for the FPGA in its application. Both ISE and Vivado ML tools provide the ability to accurately estimate the power required.

Of course, to get the most accurate power estimation, the developer needs to provide the best information. We can start our power estimation journey by using the most appropriate power estimation spreadsheets, knowing the resources required in the ISE implementation eases the power estimation for 7 series or UltraScale devices.

Within ISE, we can extract an estimation for the power required at the end of the implementation process. In the example below, this is the power required in ISE for the implementation of a Space Wire Codec.

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device			On-Chip	Power (W)	Used	Available	Utilization (%)		Supply Summary		Total	Dynamic	Quiescent
Family	Spartan6		Clocks	0.024	1	---	---		Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc6slx45t		Logic	0.003	649	27288	2		Vccint	1.200	0.086	0.036	0.049
Package	csg324		Signals	0.007	962	---	---		Vccaux	2.500	0.031	0.002	0.029
Temp Grade	C-Grade		BRAMs	0.005	*	*	*		Vcco25	2.500	0.047	0.045	0.002
Process	Maximum		DCMs	0.016	1	8	12						
Speed Grade	-3		IOs	0.146	37	190	19				Total	Dynamic	Quiescent
			Leakage	0.097					Supply Power (W)		0.297	0.162	0.136
Environment			Total	0.297									
Ambient Temp (C)	25.0												
Use custom TJA?	No		Thermal Properties		Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)						
Custom TJA (C/W)	NA				22.6	78.3	31.7						
Airflow (LFM)	0												
Heat Sink	None												
Custom TSA (C/W)	NA												
Characterization													
Production	v1.3,2011-05-04												

Figure 2 – ISE Space Wire Codec Power Estimation

When migrating the design to a 7 Series Arty S7-50, we can implement the design in Vivado ML and obtain an updated power estimation for that implementation.

This implementation predicts a lower power dissipation. However in Vivado ML, the tool reports a confidence level on its prediction. In this case the confidence level is low, which means the prediction is likely to be more pessimistic.

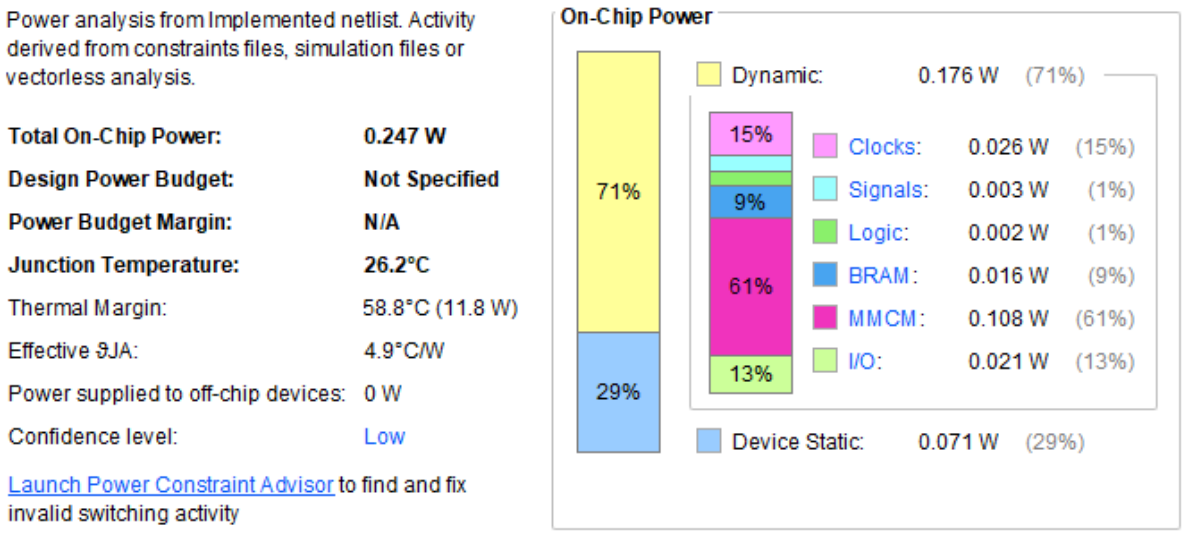

Figure 3 – Spartan 7-50 Space Wire Codec Power Estimation

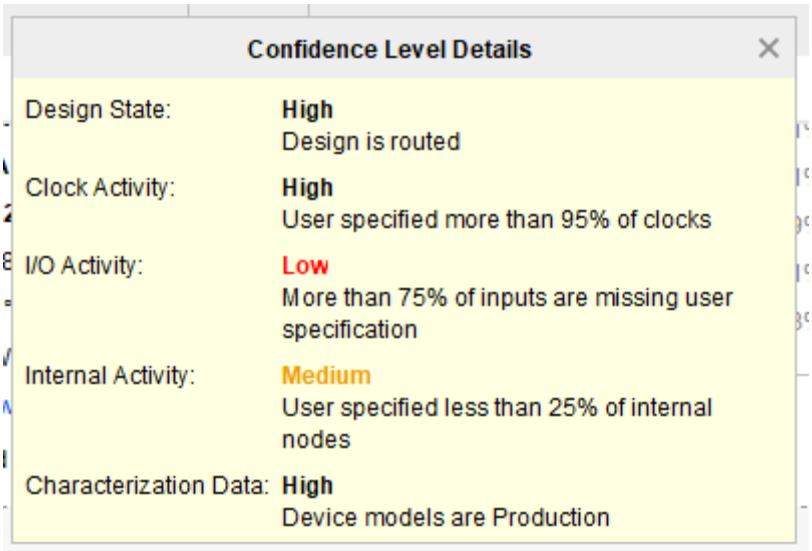

Figure 4 – Codec Power Estimation Confidence Report

To increase the accuracy of the power estimation, the IO and Internal activity can be improved by running a simulation and outputting a Switching Activity Interchange Format (SAIF). This file can be loaded into the power estimator to increase the accuracy of the overall power estimation.

A more accurate estimation enables better sizing of the power supply solution.

Clocking Networks

7 series devices provide the developer with several clocking options as each IO bank provides the user with several clock capable pins. These pins provide either the ability to clock multiple clock regions (MRCC) or single clock regions (SRCC)

MRCC pins can drive the widest range of clocking resource within the device. They can access up to three additional clocking regions using the BufR and the global clock network, while SRCC pins can access the resources of a single clock region and the global clock network. Each IO bank provides two SRCC and two MRCC pins.

Clocking Function or Pin	Directly Driven By	Used to Directly Drive
Multi-region clock-capable I/O (MRCC) There are two pin/pairs in each bank.	External Clock	MRCCs that are located in the same clock region and on the same left/right side of the device drive: • Four BUFIOs • Four BUFRs • Two BUFMRs • One CMT (one MMCM and one PLL) • CMTs above and below (using limited CMT backbone resources)(1). MRCCs within the same half top/bottom drive: • 16 BUFGs MRCCs within the same horizontally adjacent clock regions drive: • BUFHs
Single-region clock-capable I/O (SRCC) There are two pin/pairs in each bank.	External Clock	SRCCs that are located in the same clock region and on the same left/right side of the device drive: • Four BUFIOs • Four BUFRs • One CMT (one MMCM and one PLL) • CMTs above and below (using limited CMT backbone resources)(1). SRCCs within the same half top/bottom drive: • 16 BUFGs SRCCs within the same horizontally adjacent clock region drive: • BUFHs

Table 3 – Multi and Single Region Clock Capabilities

Pin Planning

Migration from Spartan-6 FPGA to 7 series and UltraScale devices comes with a need to migrate the pin out of the device. To ensure no errors can be introduced before the layout is finalised, Vivado ML tools enable developers to create a Pin Planning project.

A pin planning project enables developers to read in a CSV or XDC (Xilinx Design Constraints) file which defines the pin locations and IO standards. When migrating a design from Spartan-6 to 7 series and UltraScale devices, the IO requirements will be clearly defined from the previous Spartan-6 implementation.

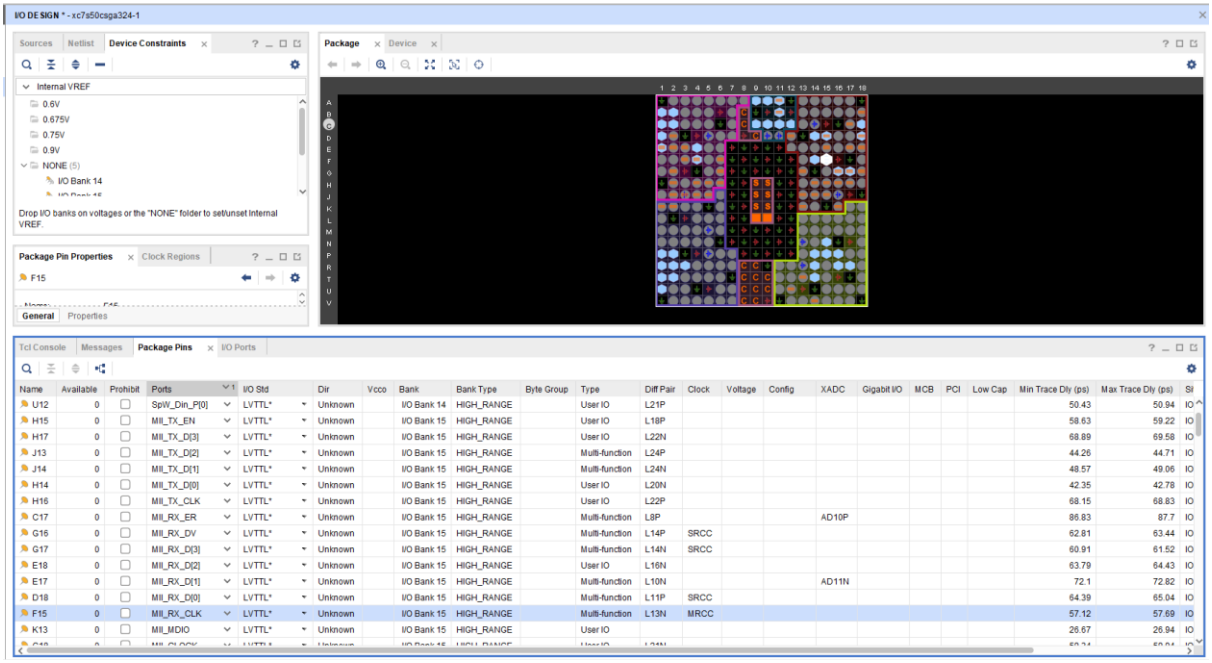

Figure 5 – Pin Planning Project in Vivado ML Tools

To help create a valid pin allocation which complies with IO Banking rules, Vivado ML tools can automatically place the I/O ports using the information provided.

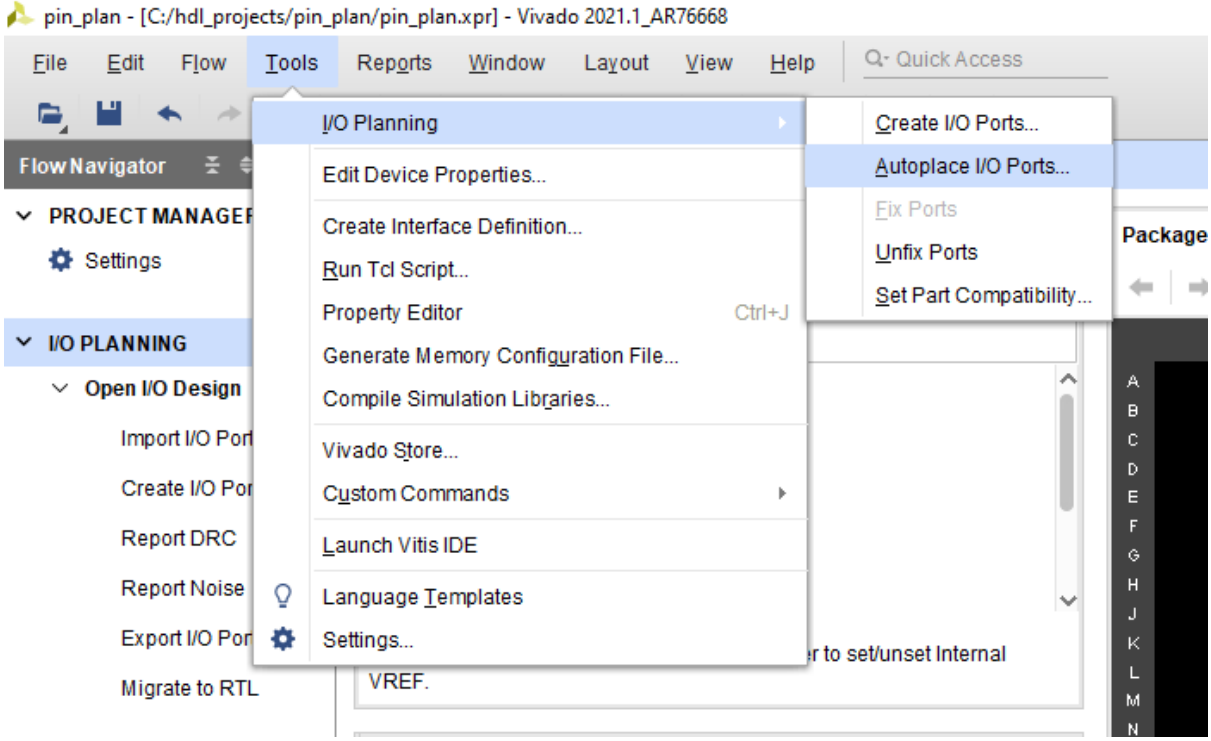

Figure 6 – Auto placing I/O Pins

To aid the development of the circuit board and especially signal integrity of the signals, both simultaneous switching outputs can be analysed and an IBIS file can be exported.

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin (%)	Notes
I/O Bank 34 (12)		multiple	1.50	FAST	multiple	FP_VTT_50		
K1	DDR3_0_dm[1]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
J1	DDR3_0_dq[8]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
L3	DDR3_0_dq[9]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
K2	DDR3_0_dq[10]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
H2	DDR3_0_dq[11]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
H1	DDR3_0_dq[12]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
M2	DDR3_0_dq[13]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
L2	DDR3_0_dq[14]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
N3	DDR3_0_dq[15]	SSTL15	1.50	FAST		FP_VTT_50	76.45	
N1	DDR3_0_dqs_p[1]	DIFF_SSTL15	1.50	FAST		FP_VTT_50	76.45	
M1	DDR3_0_dqs_n[1]	DIFF_SSTL15	1.50	FAST		FP_VTT_50	76.45	
N2	DDR3_0_reset_n	LVCMOS15	1.50	FAST	12	FP_VTT_50	76.45	

Figure 7 – Simultaneous Switching Output Report

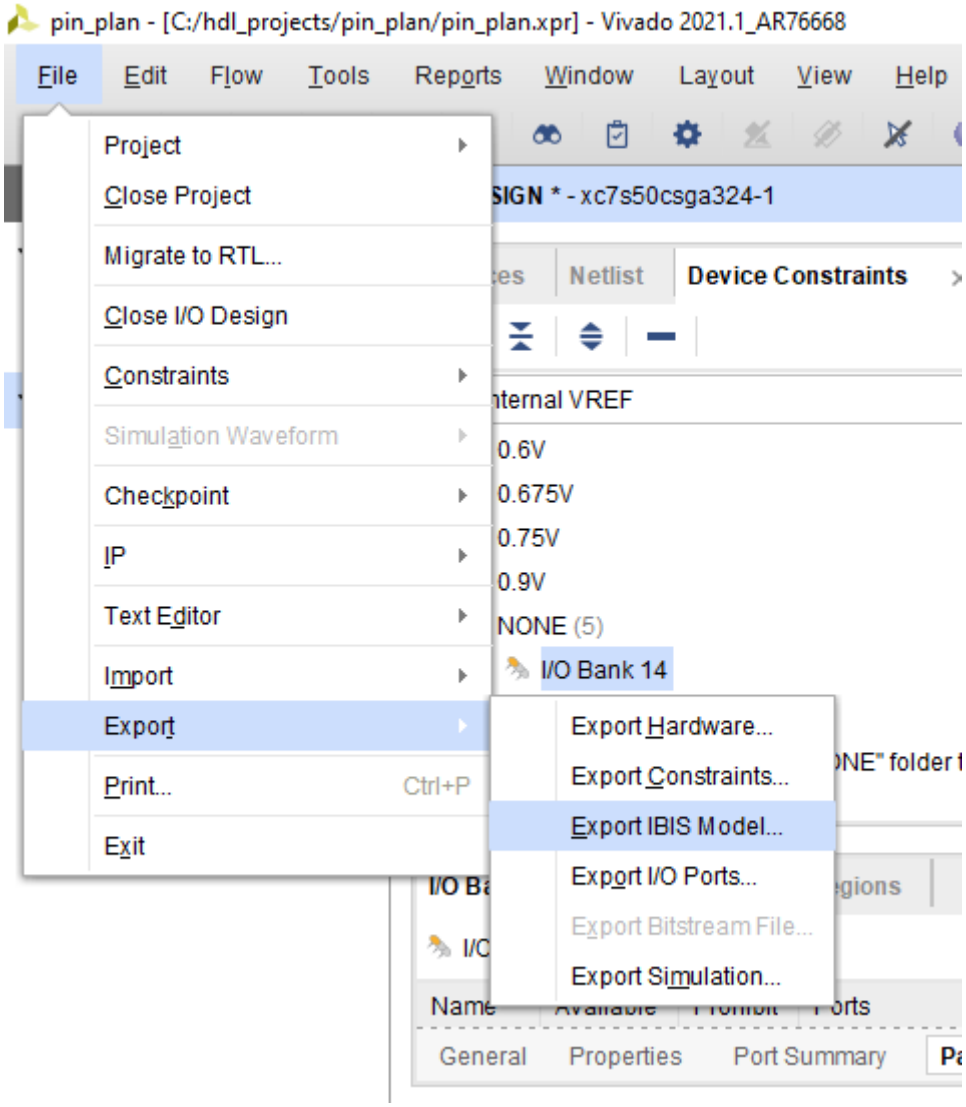

Figure 8 – Exporting the IBIS Model

As part of the migration, the opportunity may be taken to update memory interfaces, for example migrating from SDRAM to DDR.

Pin allocation for SDRAM / DDR memories is quite different between Spartan-6 and 7 series devices. Spartan 6 devices have a hard macro memory controller implemented in the silicon. This means the pin allocation for SDR/DDR is fixed and the developer must make appropriate connections in the schematic.

7 series devices use softcore memory controller which can be implemented on any IO bank.This however means the pinout is more flexible and there is a possibility of the developer making an incorrect connection.

To ensure this cannot be the case when developing 7 series solutions which use DDR memories Vivado ML provides the developer with the ability to assign address, control, and data signals when the memory interface generator is used.

For new designs in Vivado ML, the memory interface generator enables allocation of signal groups to banks.

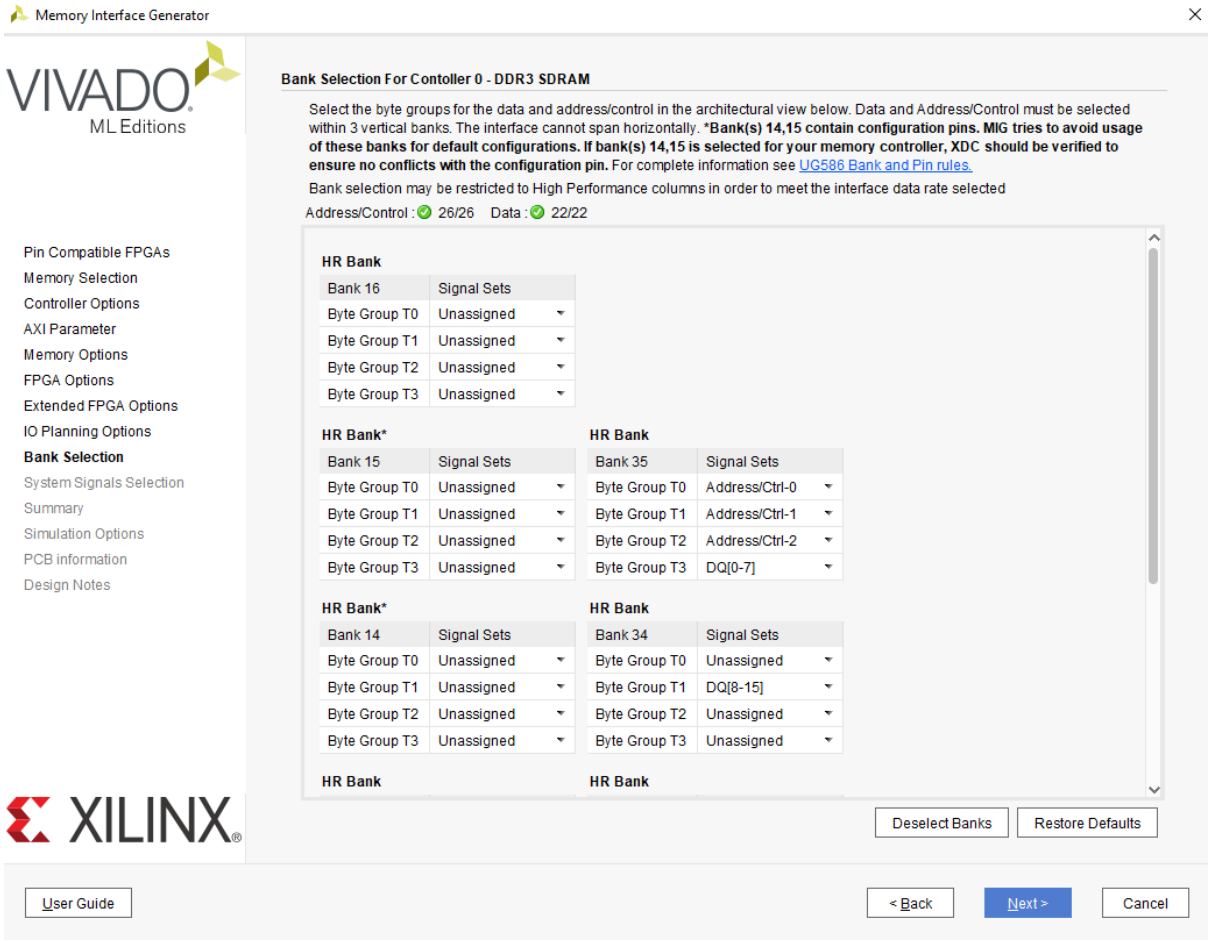

Figure 9 – Assigning Signals to Banks in Vivado ML Memory Interface Generator

These pins will be fully elaborated and allocated as the design is synthesised, ensuring a valid pin out can be used with confidence.

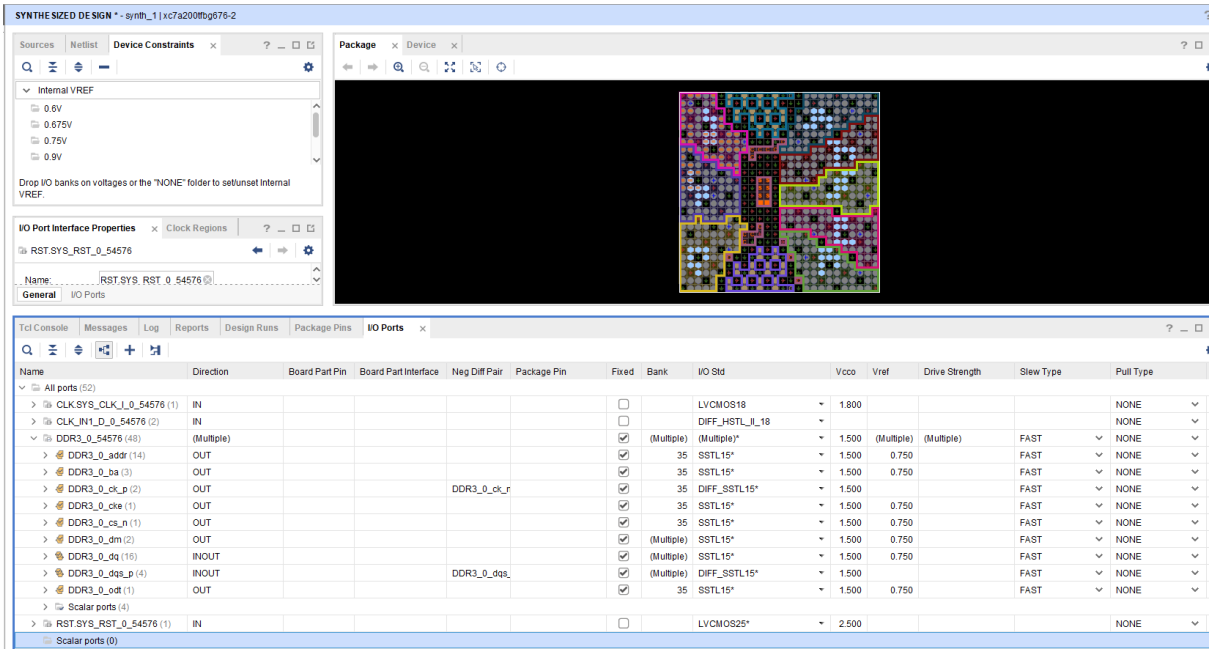

Figure 10 – Allocation of Exact DDR IO pins in Synthesised View

Conclusion

This white paper has focused on the elements required to design in a 7 series or UltraScale device into the circuit board to replace a Spartan-6 device. The stages include identification of the correct device and package, ensuring sufficient IO banks are available across the High Range and High Performance banks. With the packaging selected the next stage is estimation of the power consumption and creation of the power architecture which follows the necessary power sequence. Once that has been completed, the global clocking pins and IO allocation can take place, including the allocation of specialist pins required for DDR memory interfaces.

Following this approach enables the developer to create a schematic and PCB (Printed Circuit Board) solution which migrates a Spartan-6 design to 7 series or UltraScale devices.

Adivuo is a Xilinx Alliance Partner and has extensive experience in Xilinx designs. Contact us if you need any Spartan-6 conversion assistance.