DFX Lab

Course Workbook

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About this Workbook

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

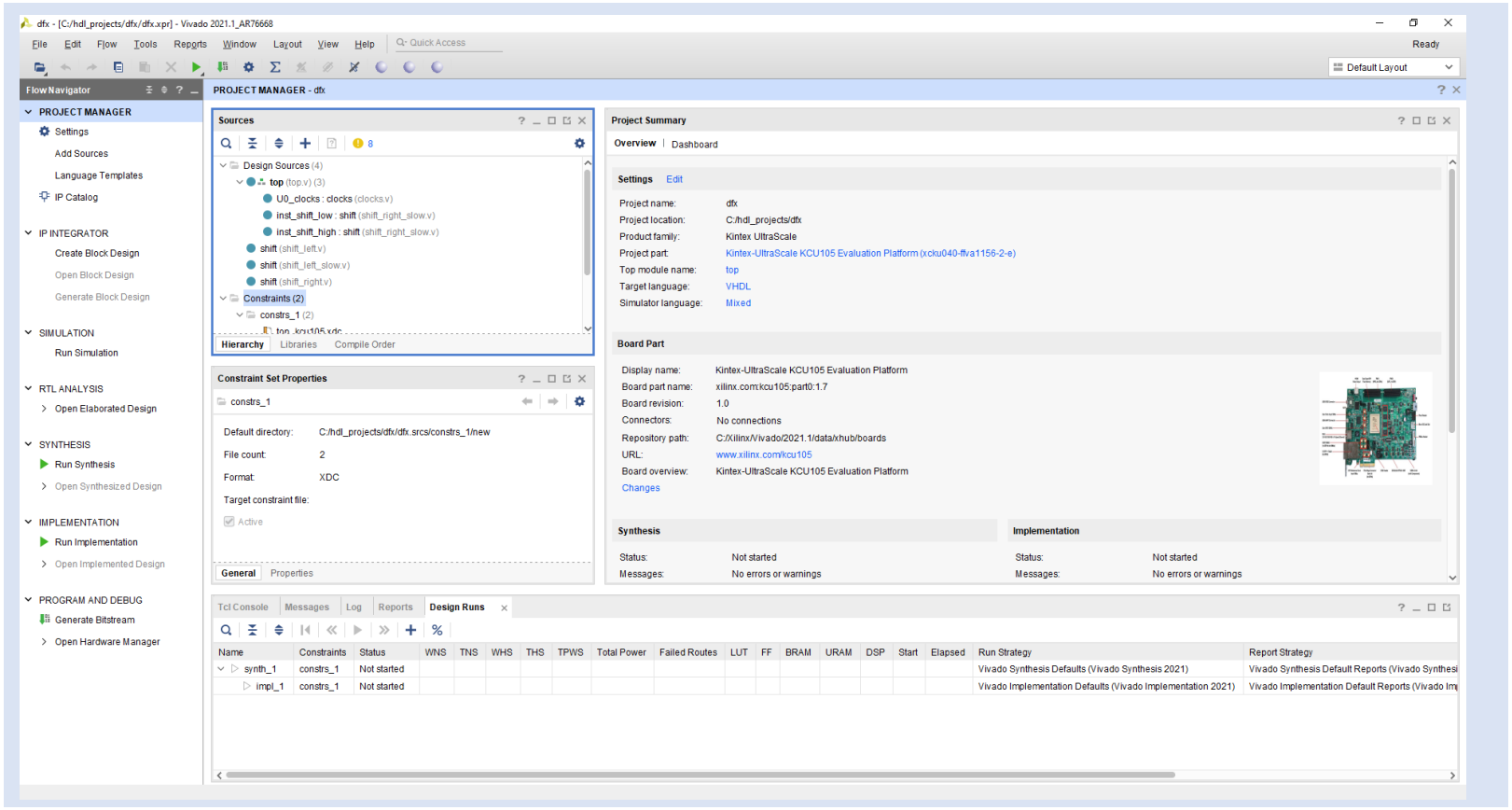
Vivado 2021.1	Download

Lab

DFX – RTL

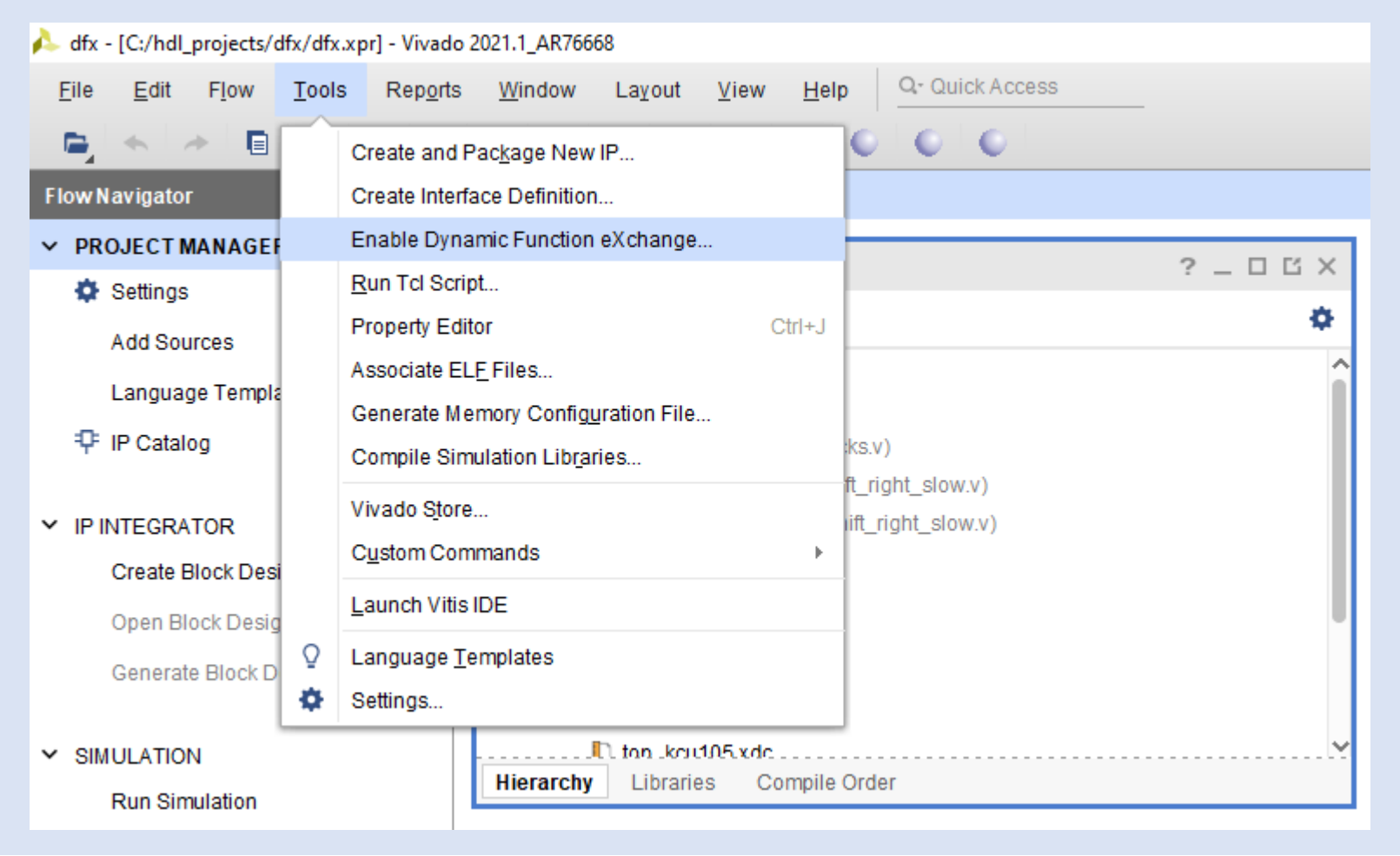
Lab: DFX

Step 1 – Download the source files from the repo creating a new project for the target board. Add to the files the constraints and the source files in the folder top.



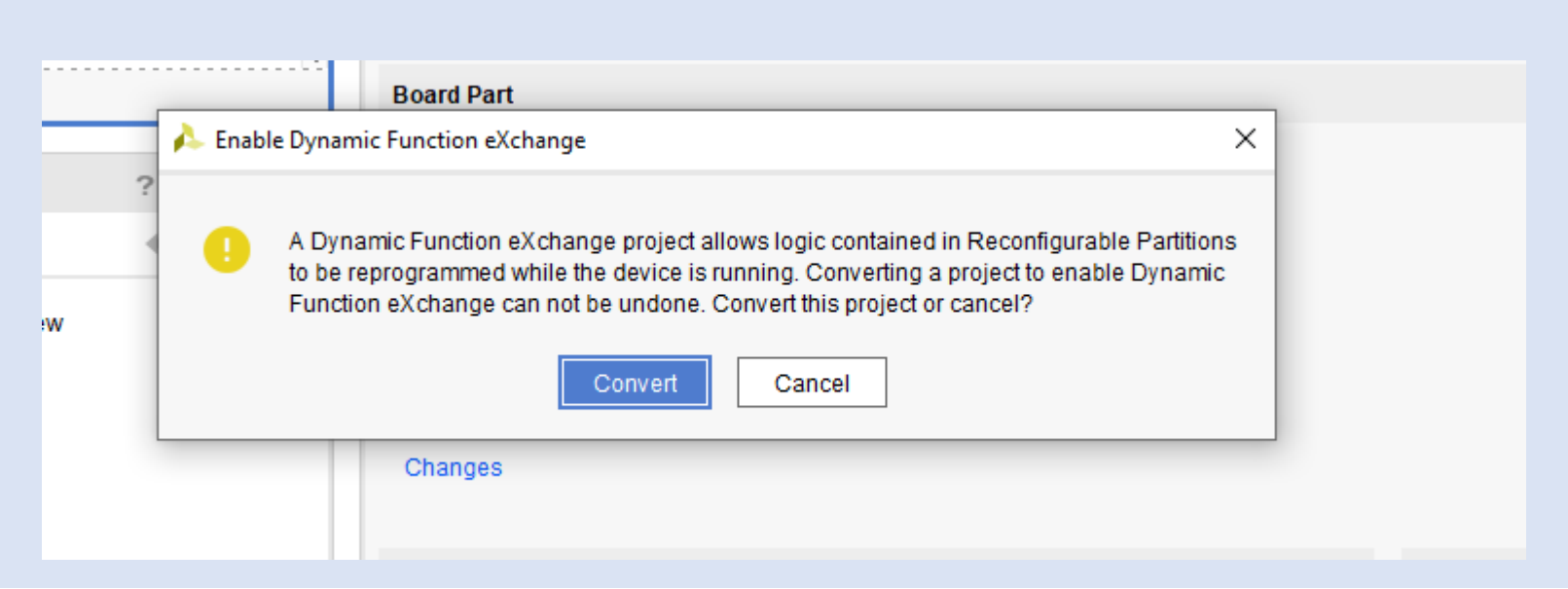
Lab: DFX

Step 2 – From the Tools menu Enable Dynamic Functional eXchange



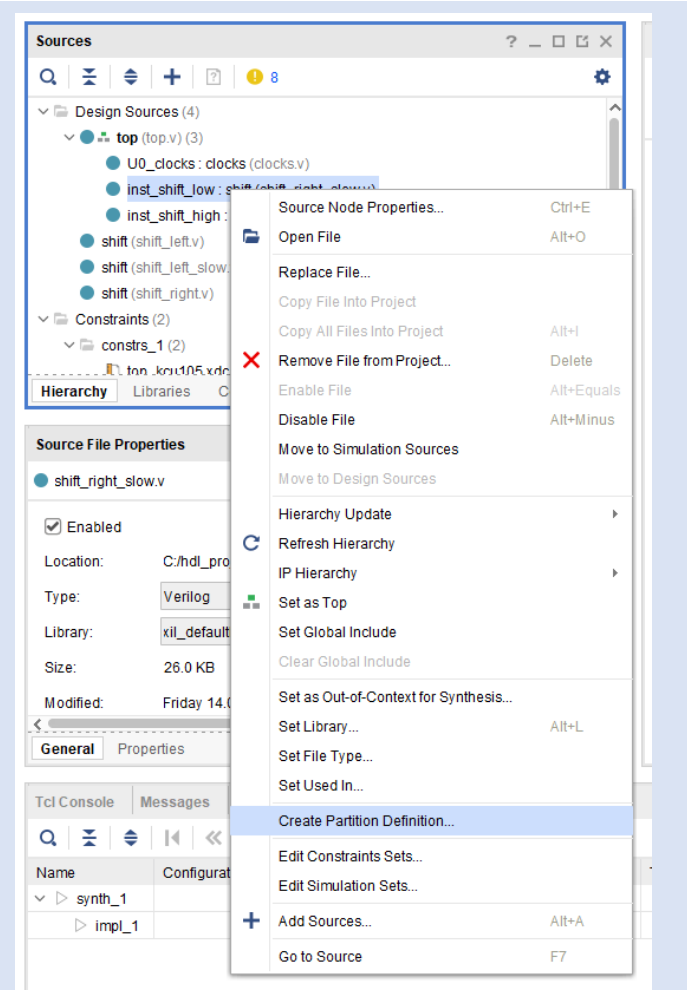
Lab: DFX

Step 3 – When prompted select convert



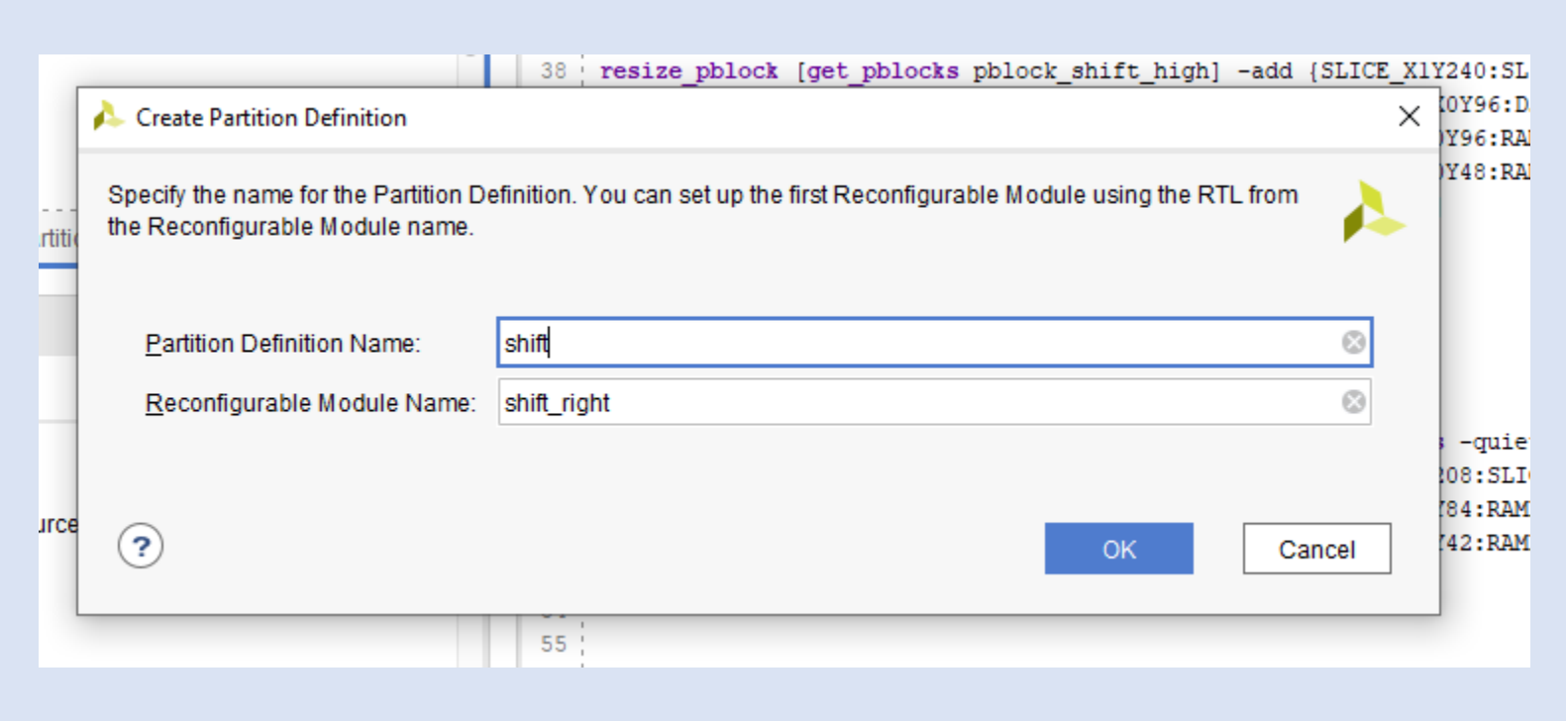
Lab: DFX

Step 4 – Select the first of the shift instances and select create partition definition



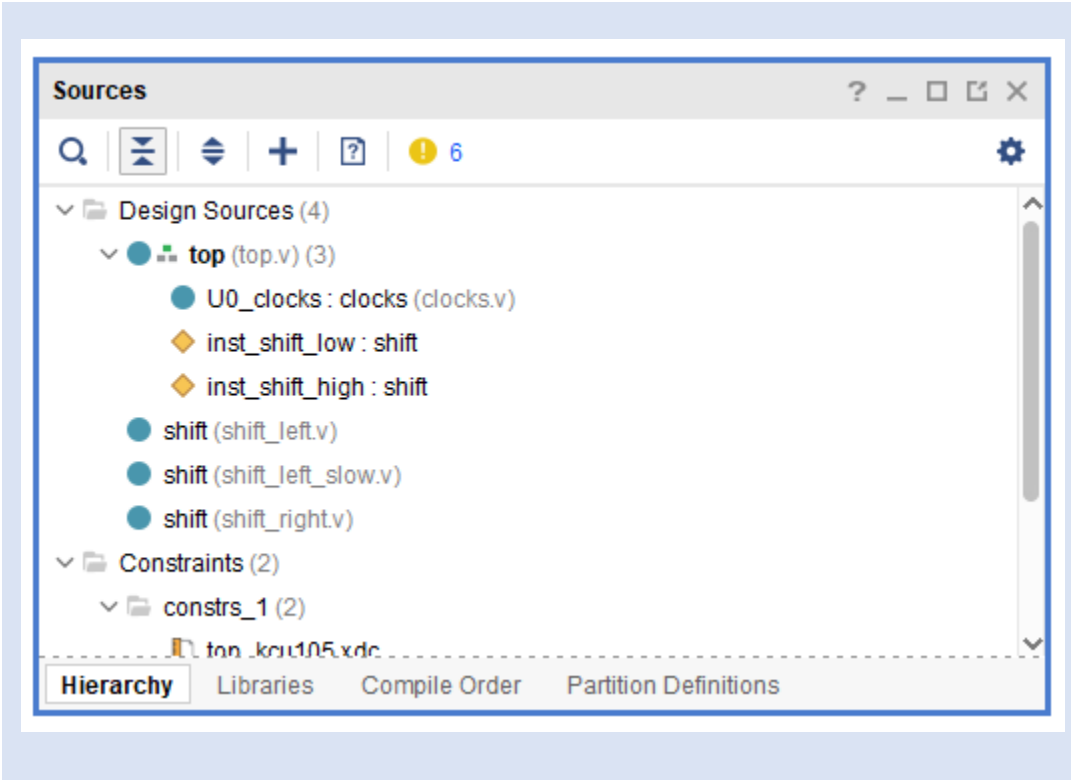
Lab: DFX

Step 5 – Enter a partition definition name and click ok



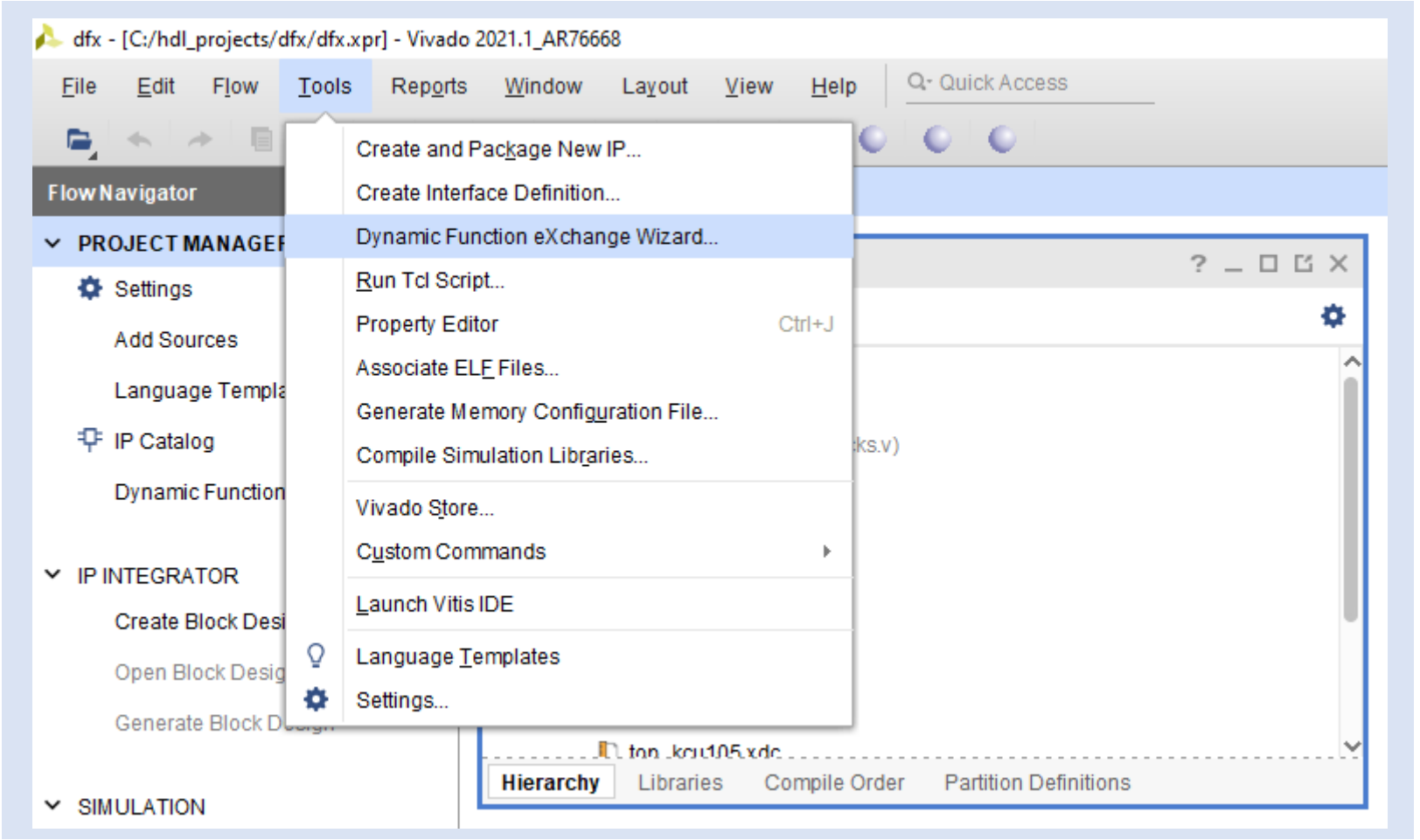
Lab: DFX

Step 6 – Note in the sources view both have changed, this is because they are the same module instantiated twice.



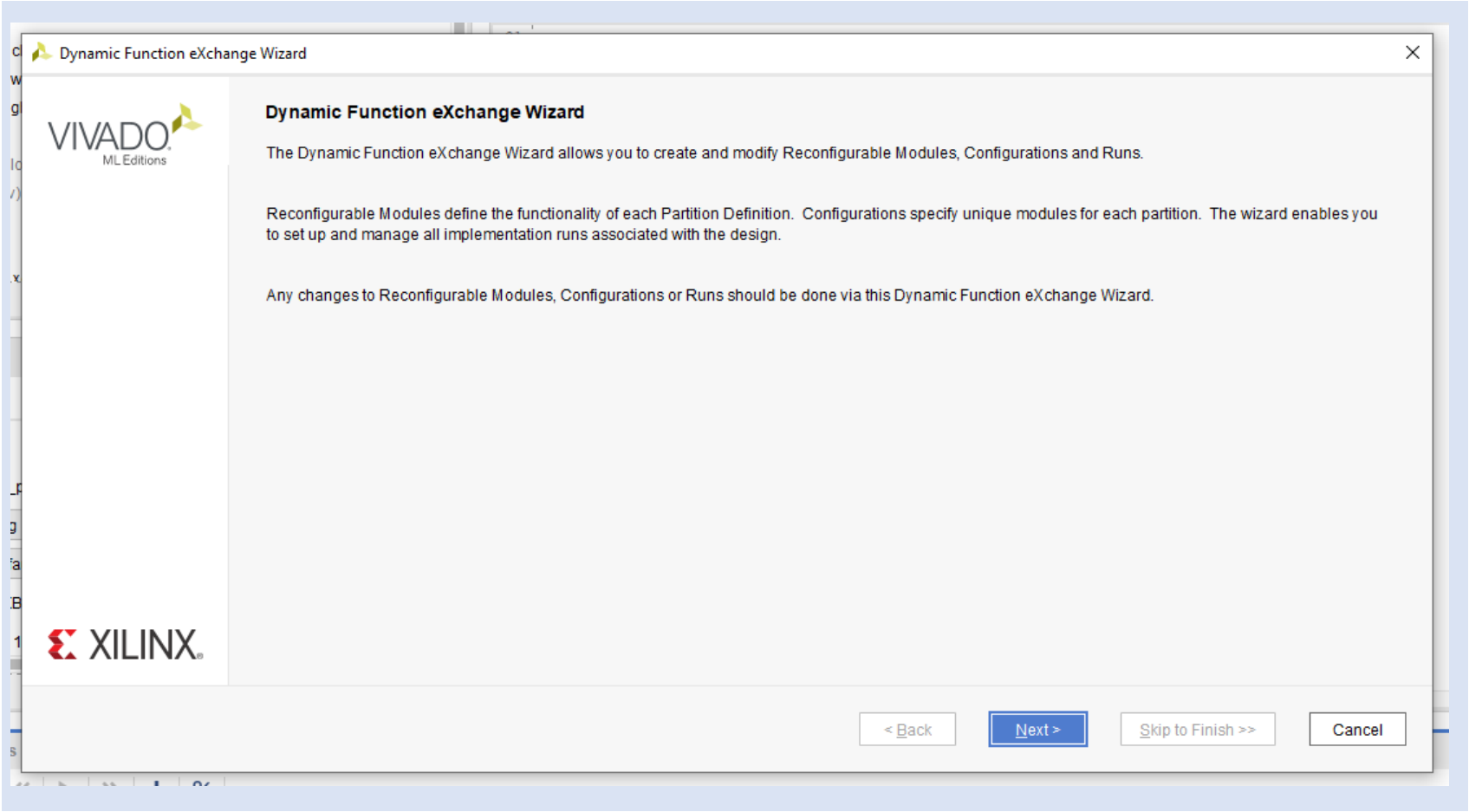
Lab: DFX

Step 7 – From the tool's menu select Dynamic Functional eXchange Wizard



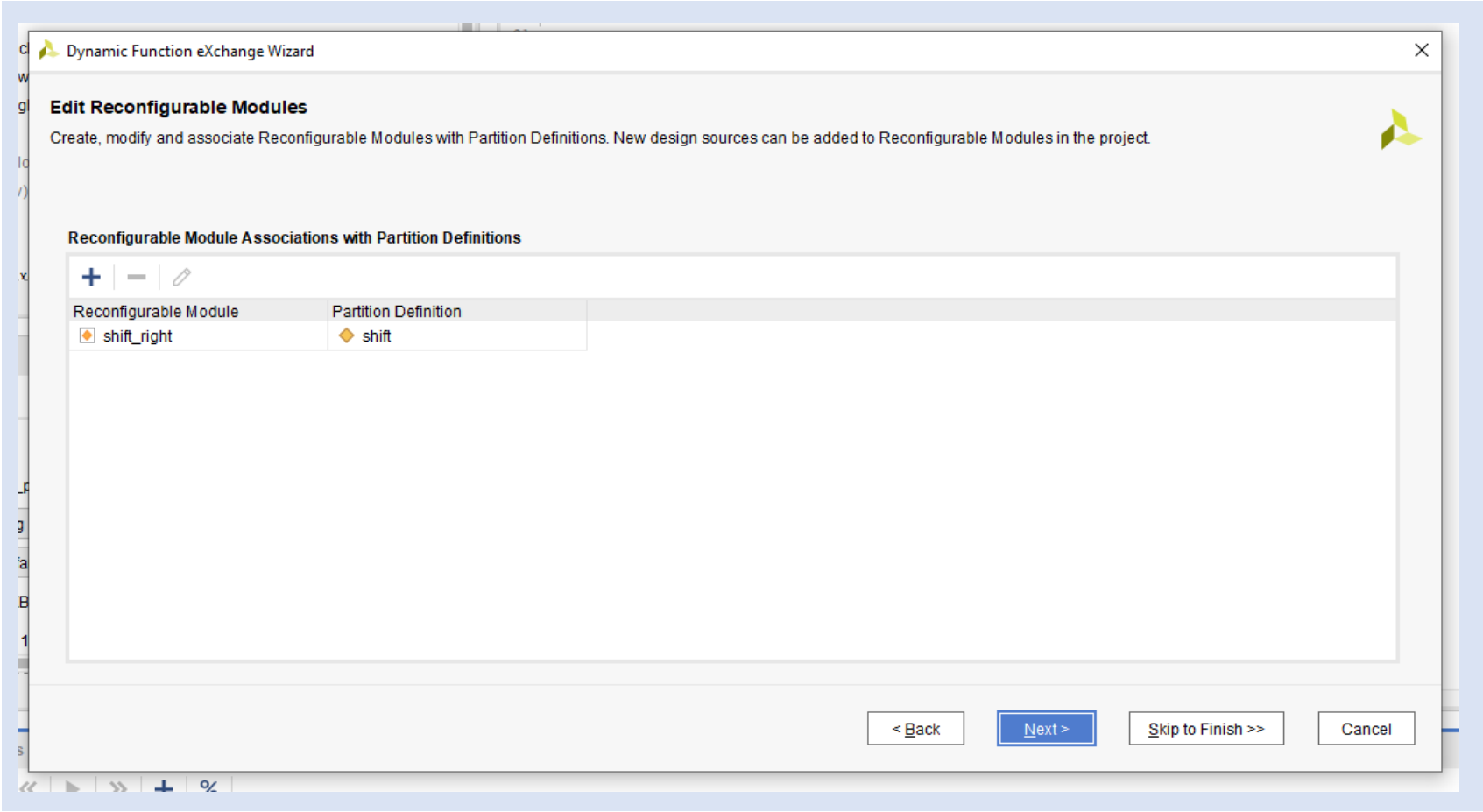
Lab: DFX

Step 8 – Click on next



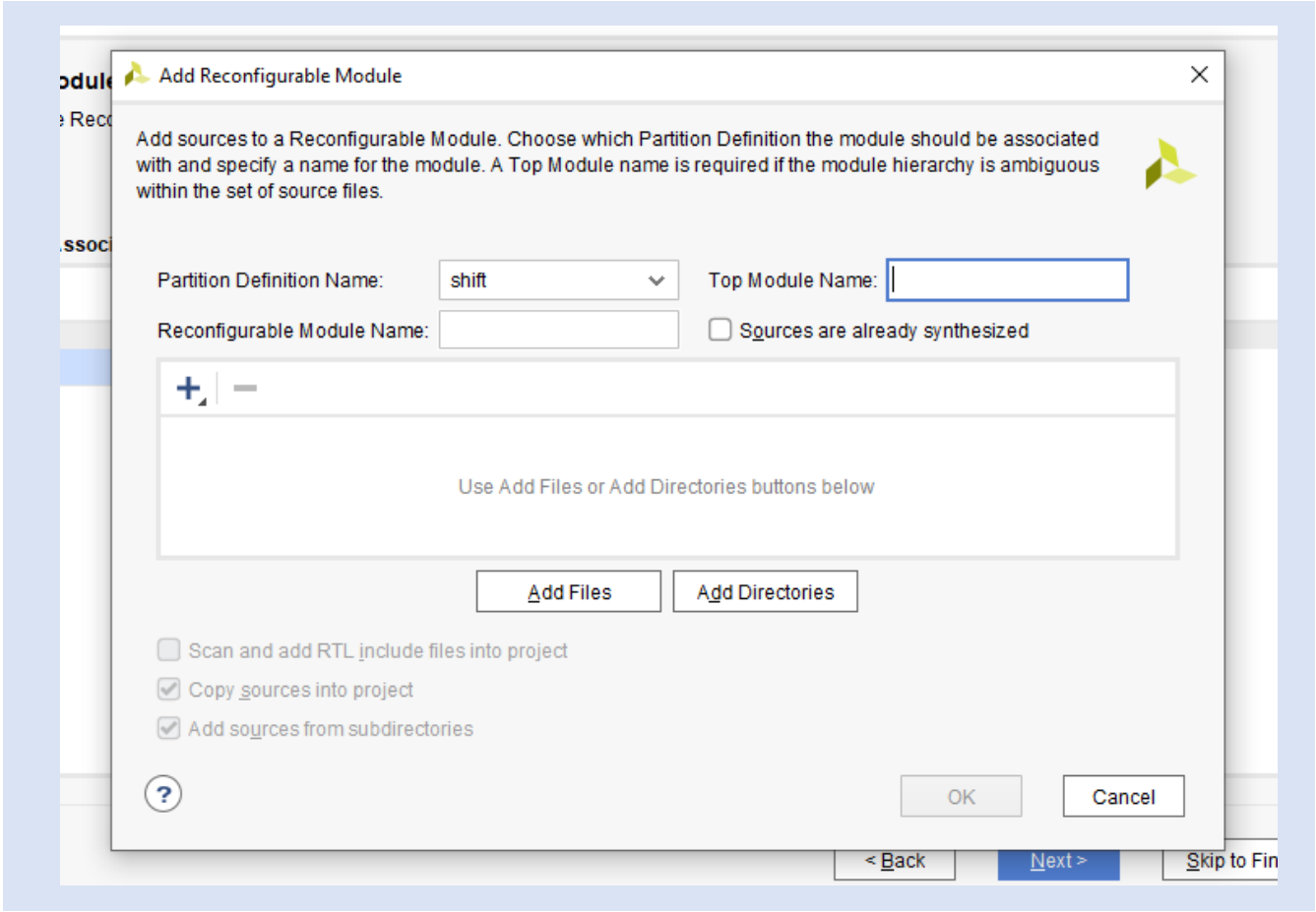
Lab: DFX

Step 9 – We can see the primary design – which will do a shift right pattern. This will be placed into the top-level bit file. We can create additional partitions by clicking on the blue +



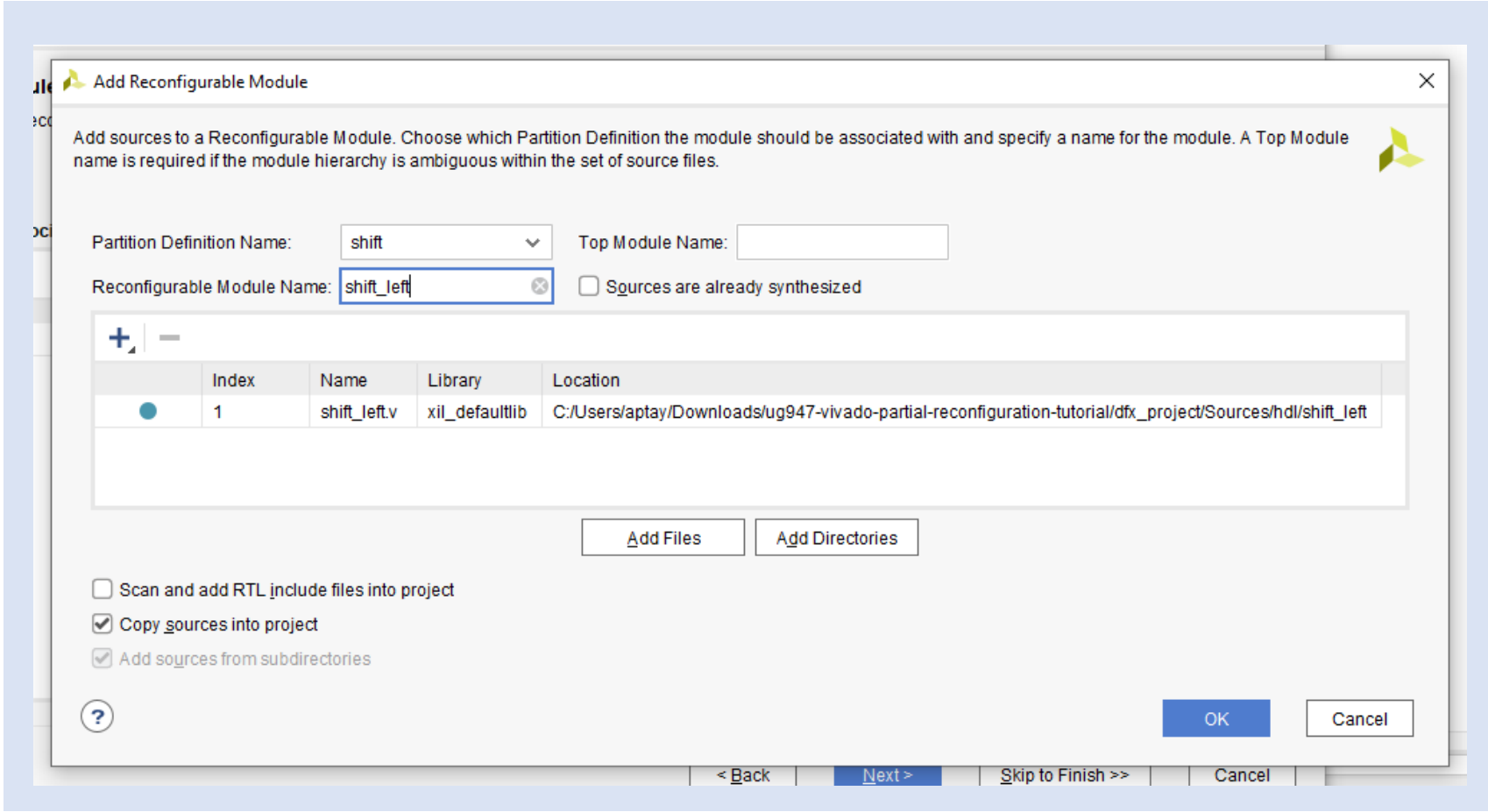
Lab: DFX

Step 10 – Click the + to add a new reconfigurable module.



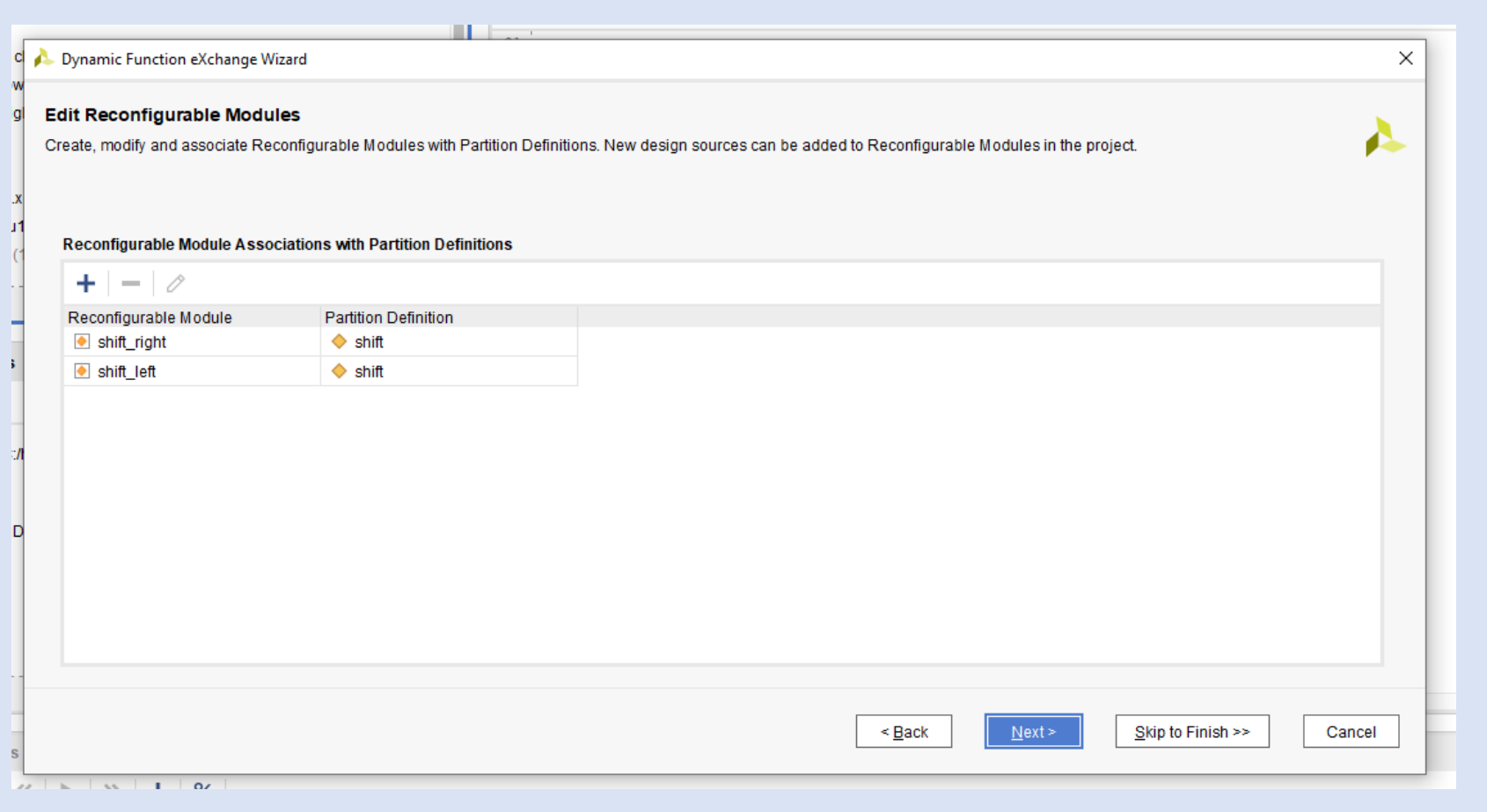
Lab: DFX

Step 11 – Add the shift_left file from the repo set the partition to shift and the reconfigurable name to shift left.



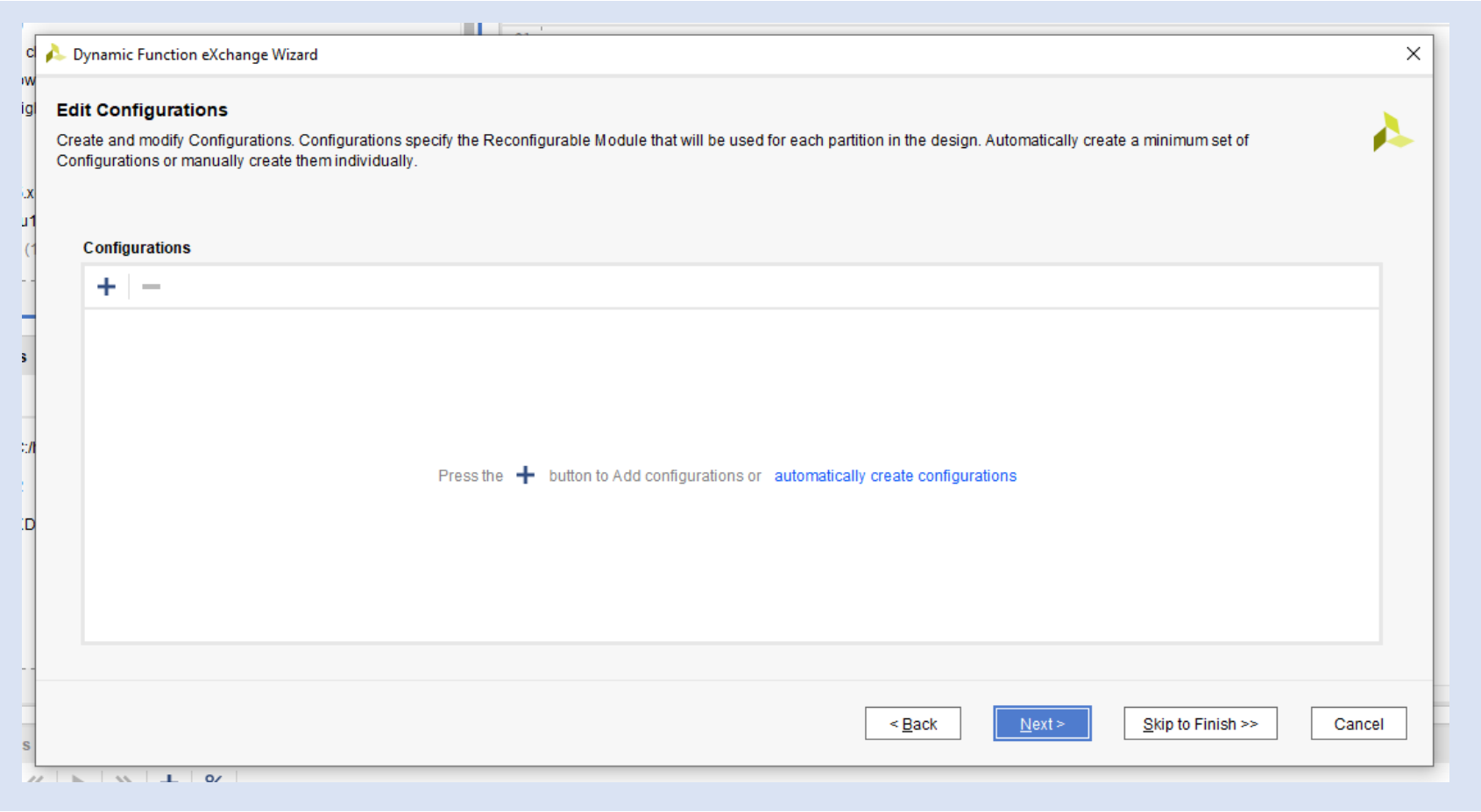
Lab: DFX

Step 12 – This will create the reconfigurable partition for the shift left pattern as well as shift right



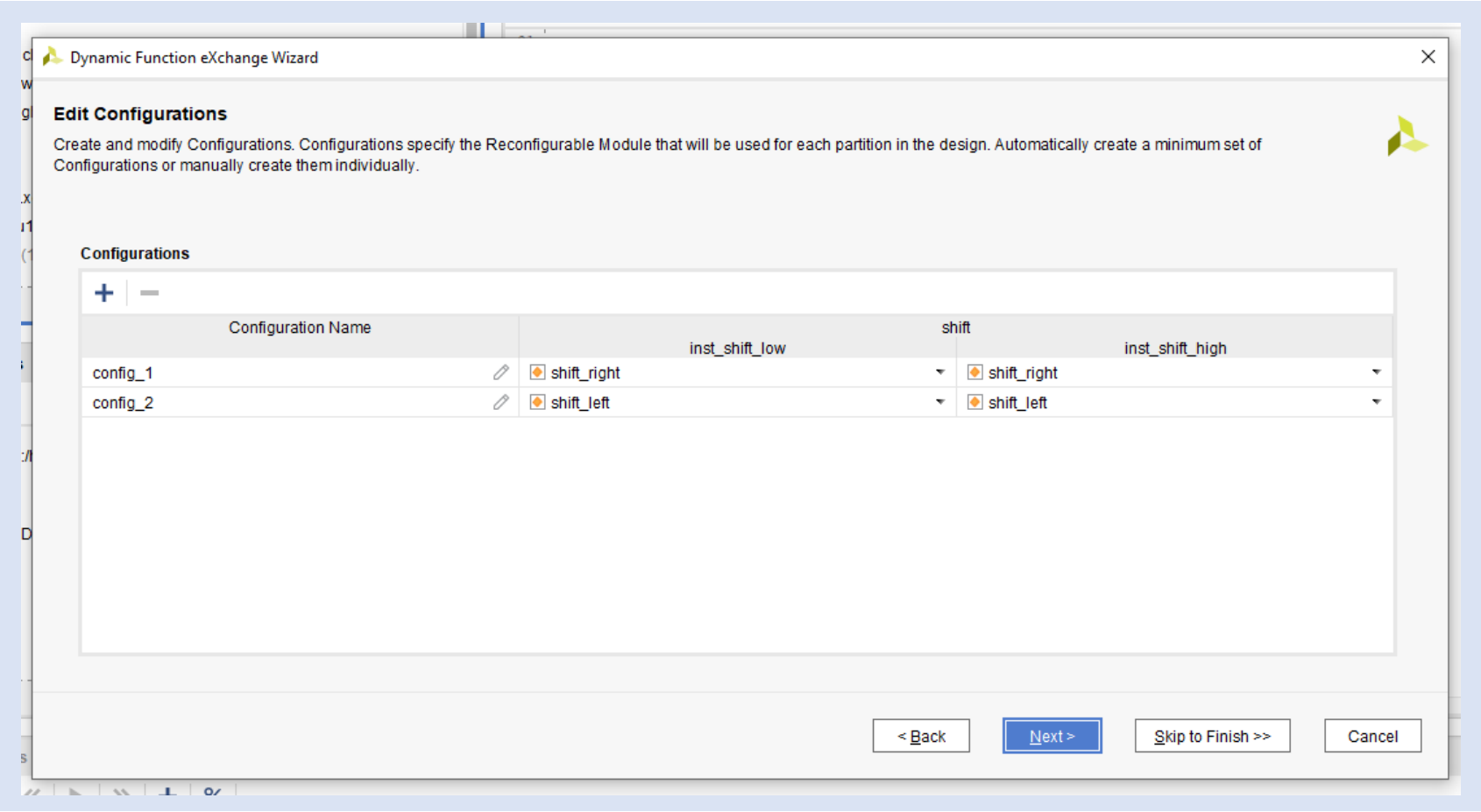
Lab: DFX

Step 13 – Click automatically create configurations



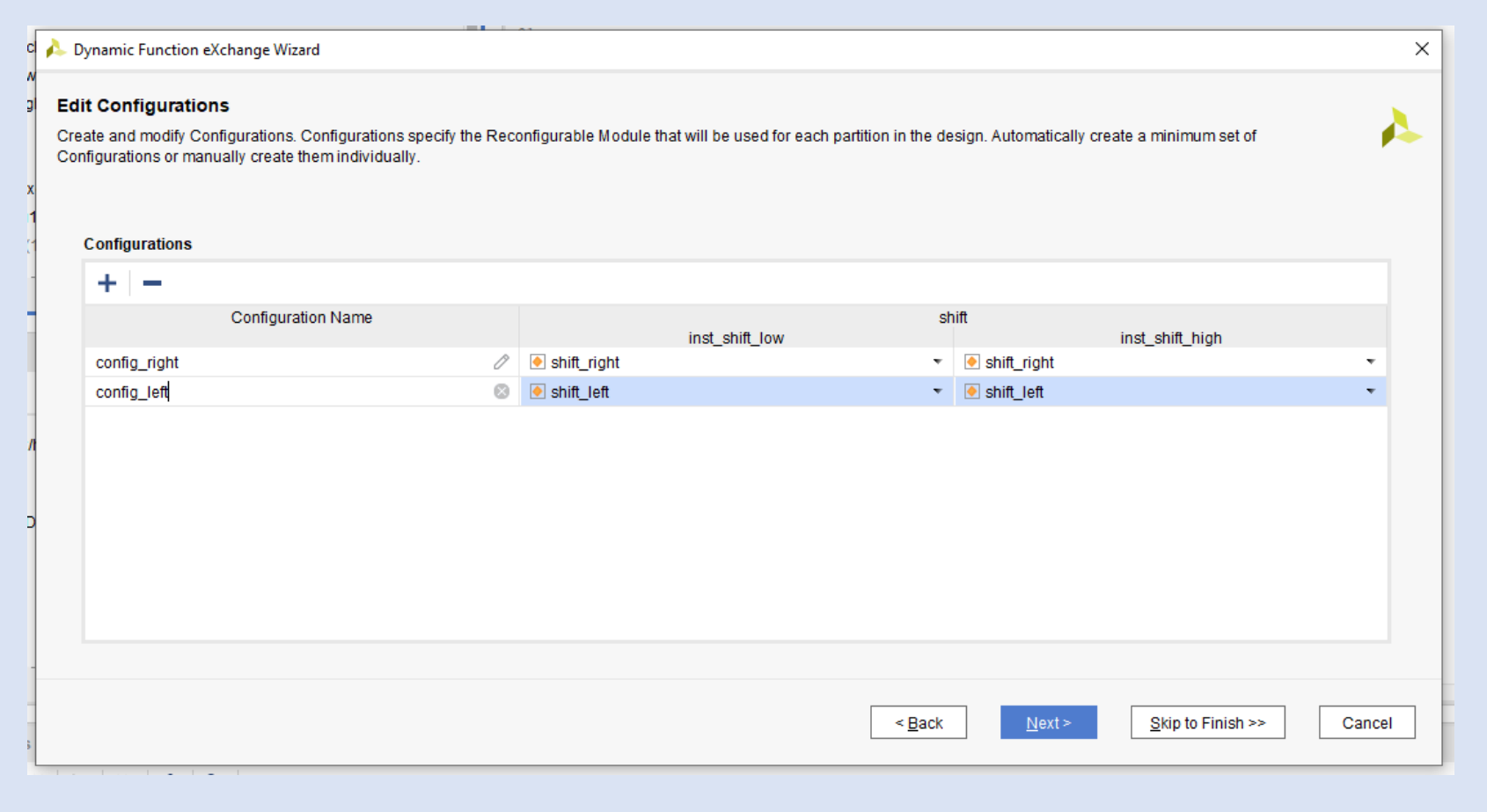
Lab: DFX

Step 14 – Once the configurations are created, use the edit feature to name the config_left and config_right



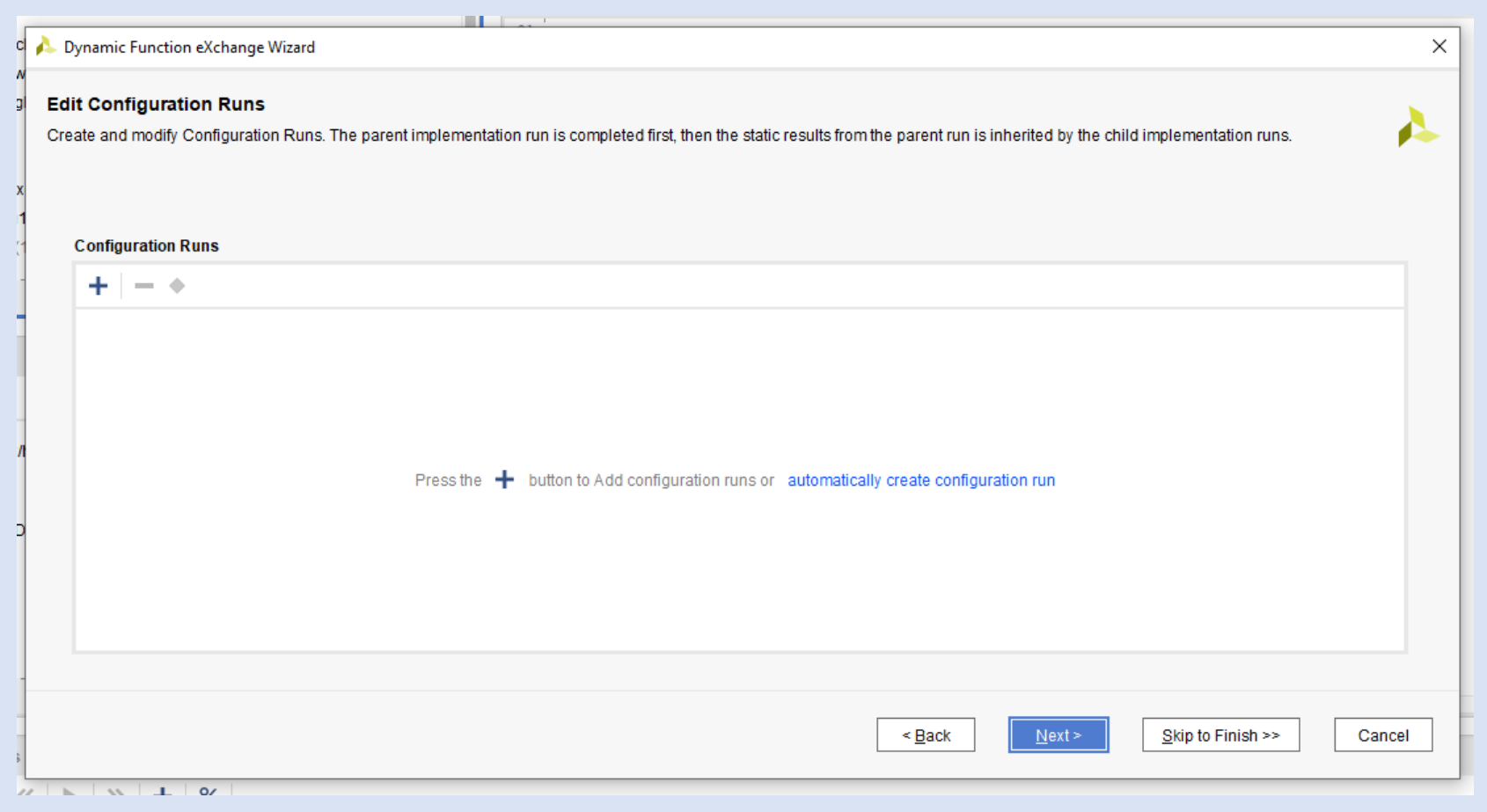
Lab: DFX

Step 15 – Click next once the modules are renamed



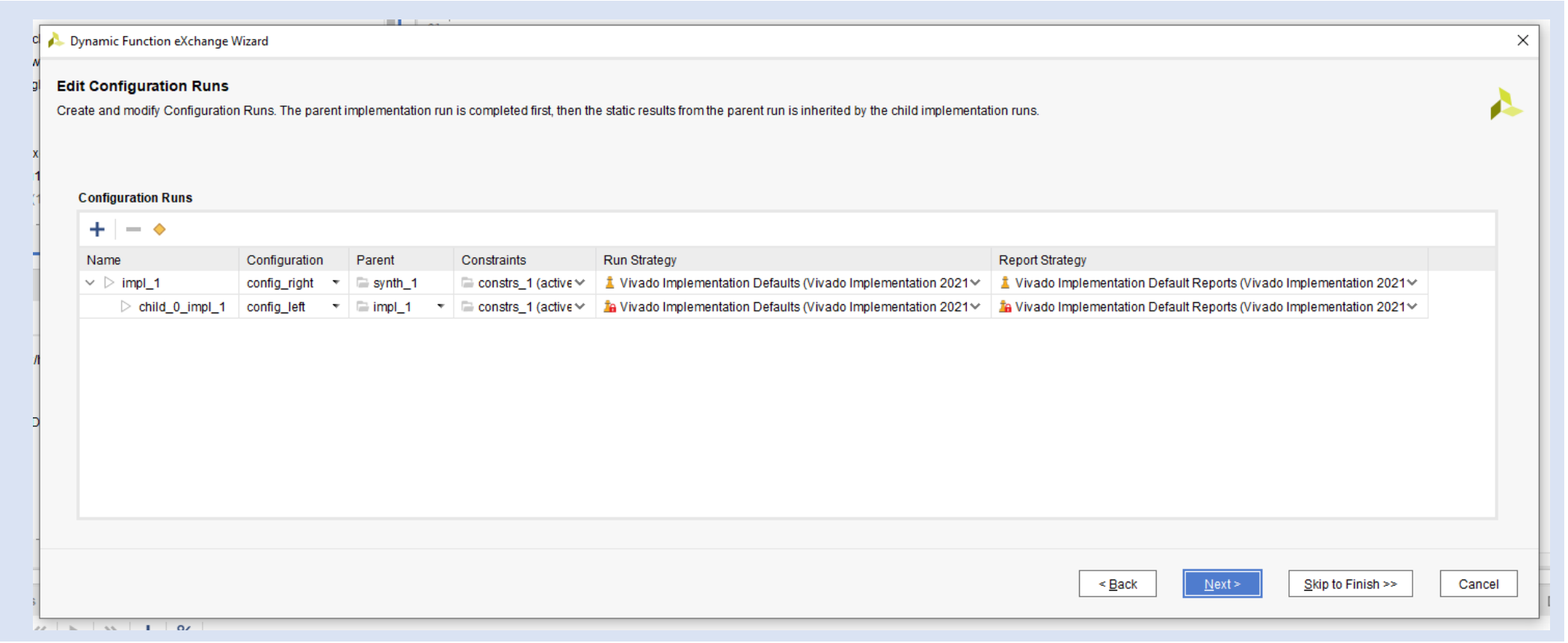
Lab: DFX

Step 16 – Click on automatically create configuration run



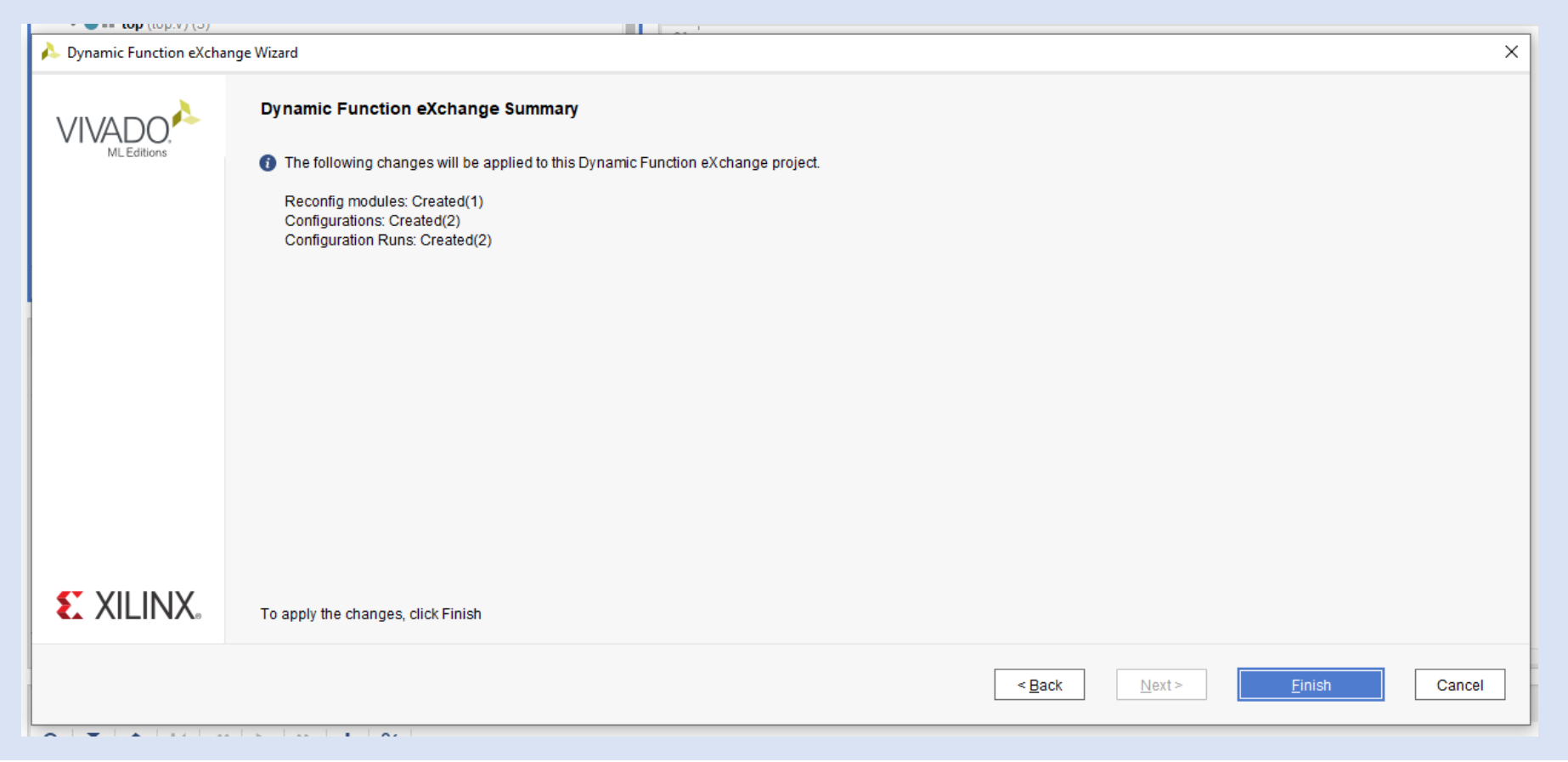
Lab: DFX

Step 17 – Once the runs have been created you will see the parent and child configurations. The child configurations are the partial reconfiguration zones. Under the configuration you can change the initial design region contents, if you desire.



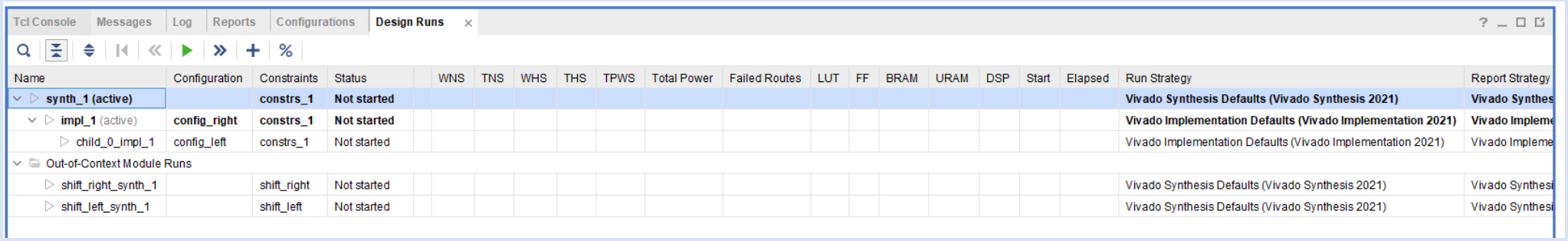
Lab: DFX

Step 18 – Click finish, this should have created the runs necessary to create the top level design and the child partial reconfiguration zones.



Lab: DFX

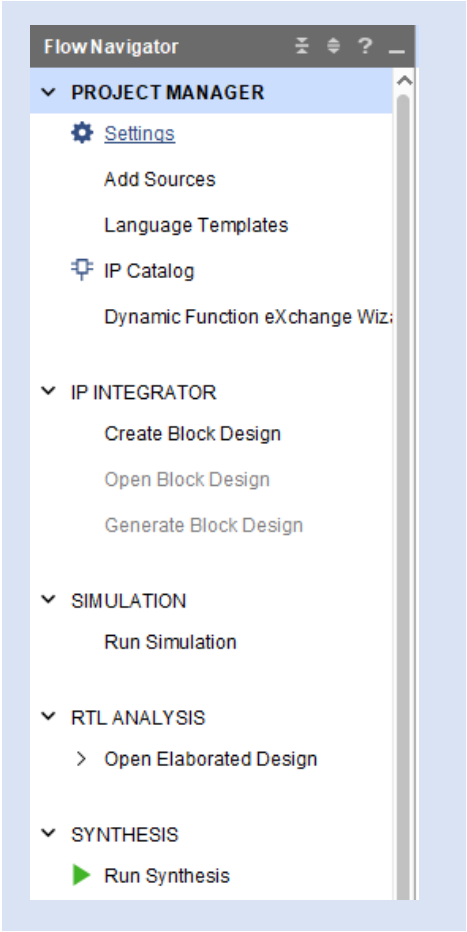
Step 19 – Observe the confirmation of the design runs, two RTL modules for OOC synthesis and one implementation set to the configuration selected and a child configured to the other configuration for the partial bit stream.



Name	Configuration	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1 (active)		**constrs_1**	**Not started**															**Vivado Synthesis Defaults (Vivado Synthesis 2021)**	**Vivado Synthes**
impl_1 (active)	**config_right**	**constrs_1**	**Not started**															**Vivado Implementation Defaults (Vivado Implementation 2021)**	**Vivado Impleme**
child_0_impl_1	config_left	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2021)	Vivado Impleme
Out-of-Context Module Runs																			
shift_right_synth_1		shift_right	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2021)	Vivado Synthesi
shift_left_synth_1		shift_left	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2021)	Vivado Synthesi

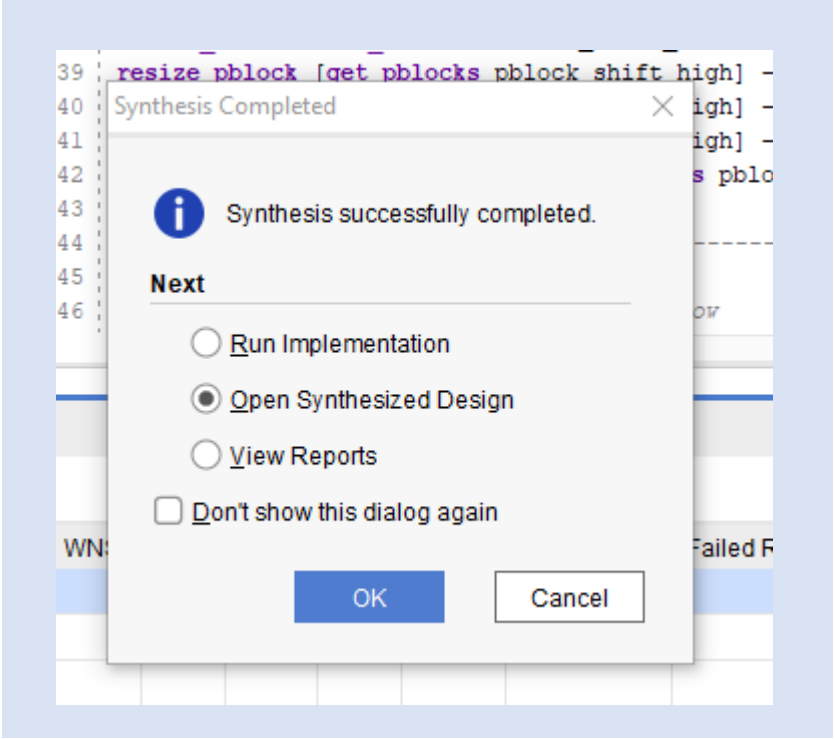
Lab: DFX

Step 20 – Run the synthesis



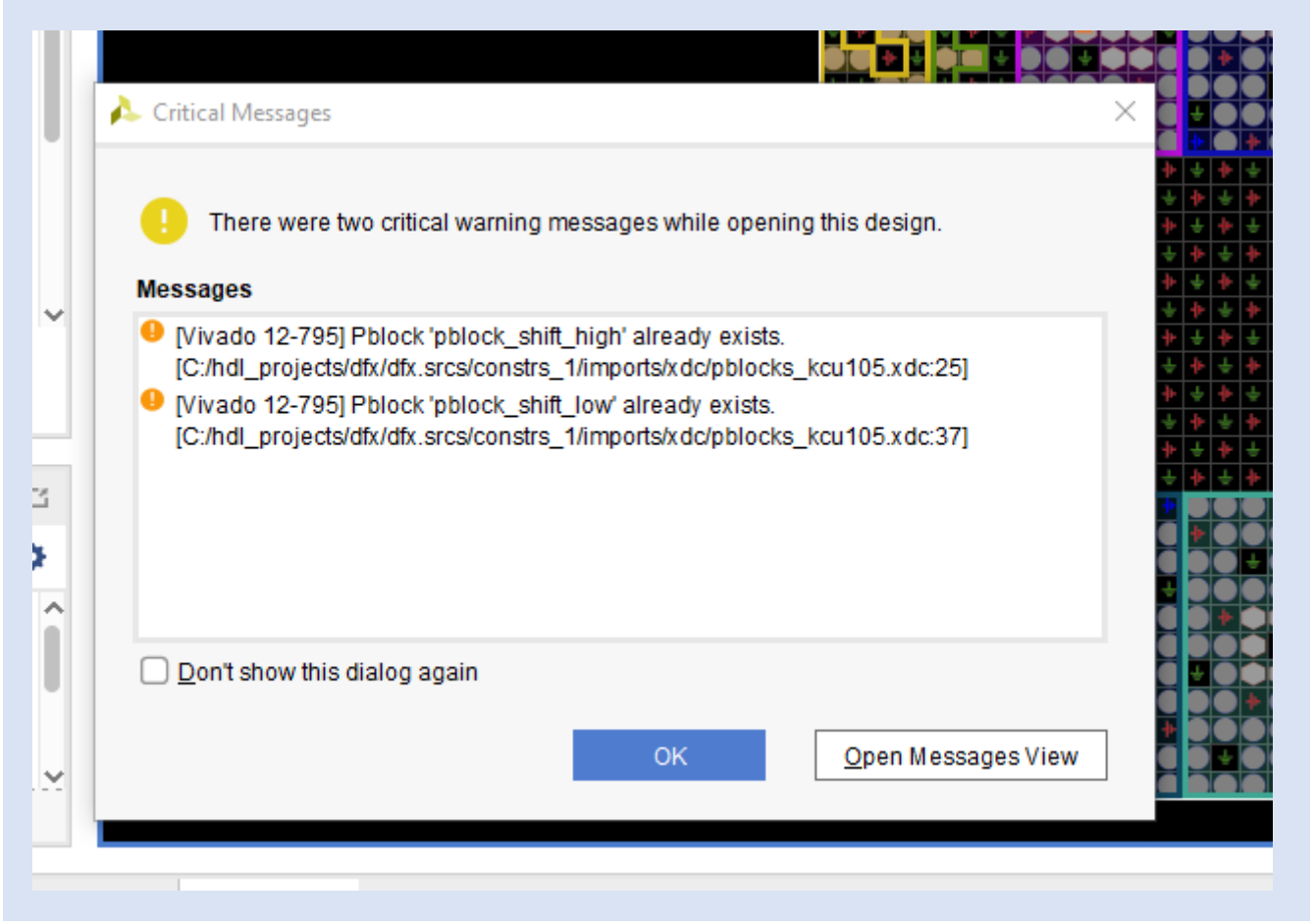
Lab: DFX

Step 21 – Open the Synthesis view when completed



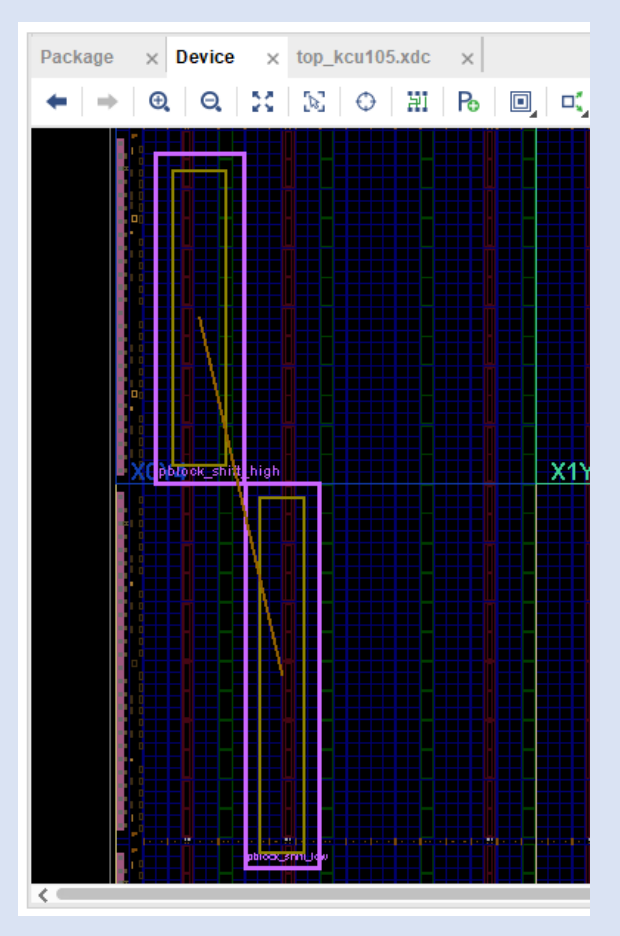
Lab: DFX

Step 22 – If the following warning appears click OK



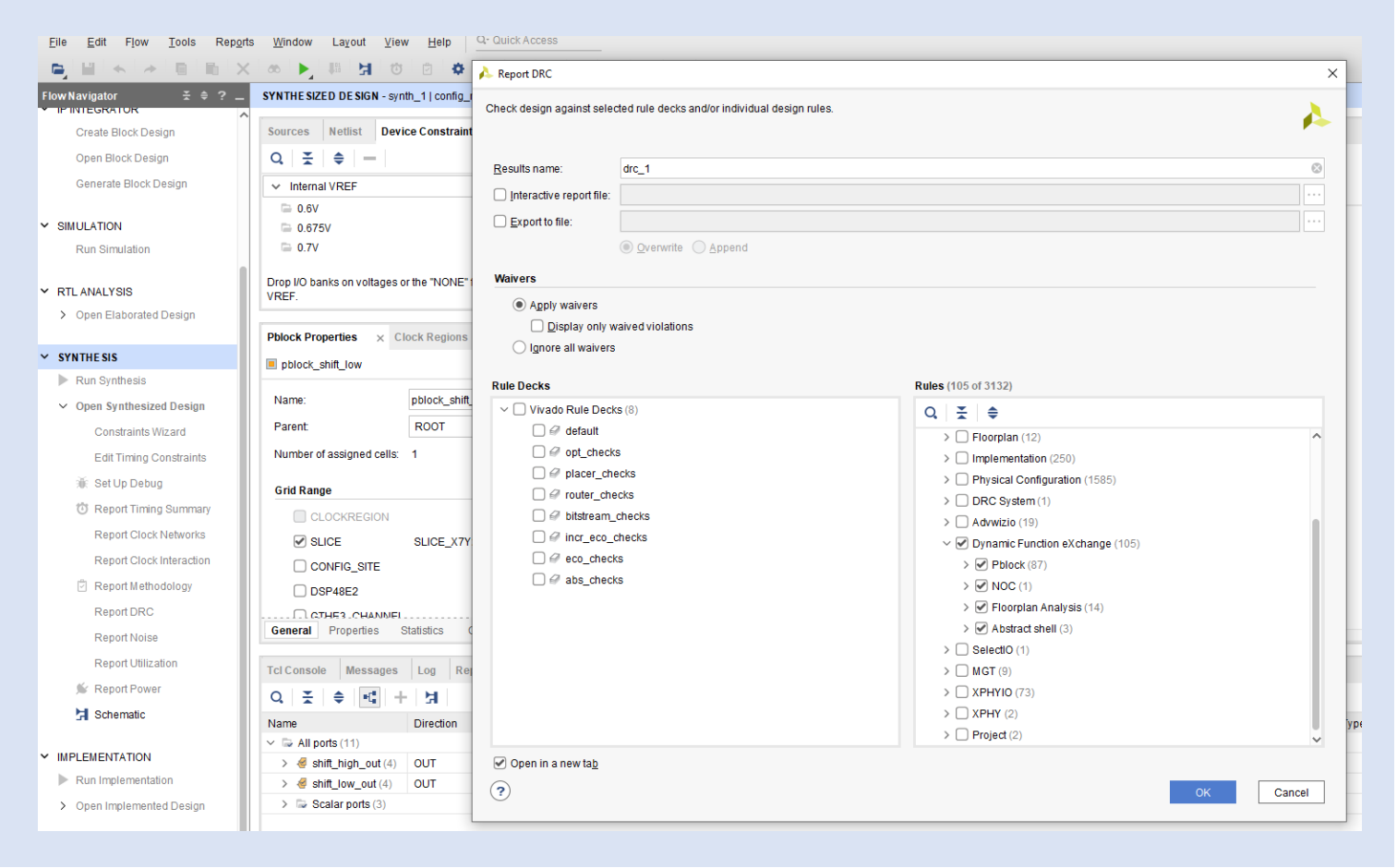
Lab: DFX

Step 23 – In the synthesis view you should see the Pblocks with the functions associated with them – this is like an Isolation flow approach.



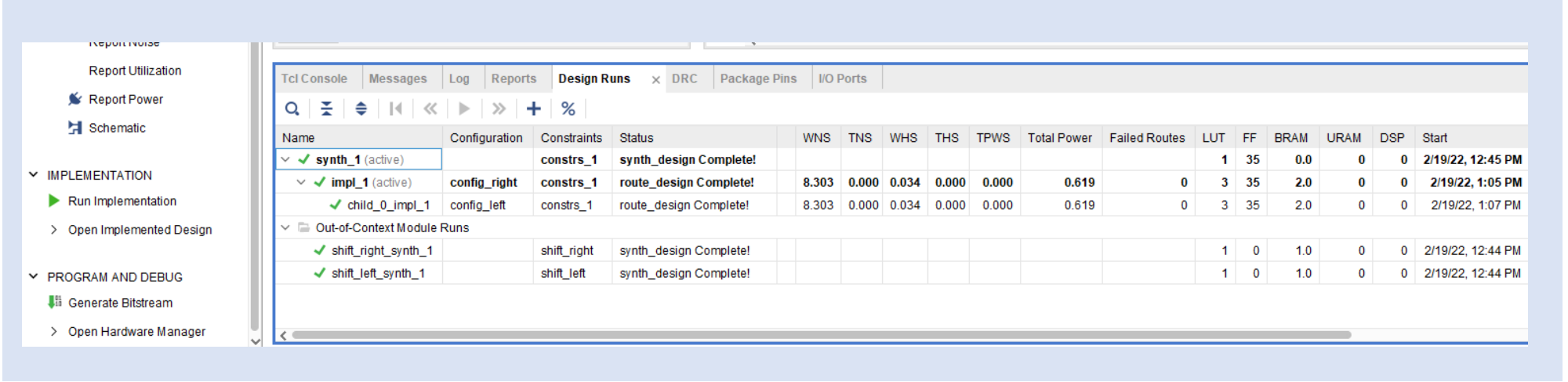
Lab: DFX

Step 24 – From the reports option run the DRC to ensure the Pblocks are OK for the partial reconfiguration



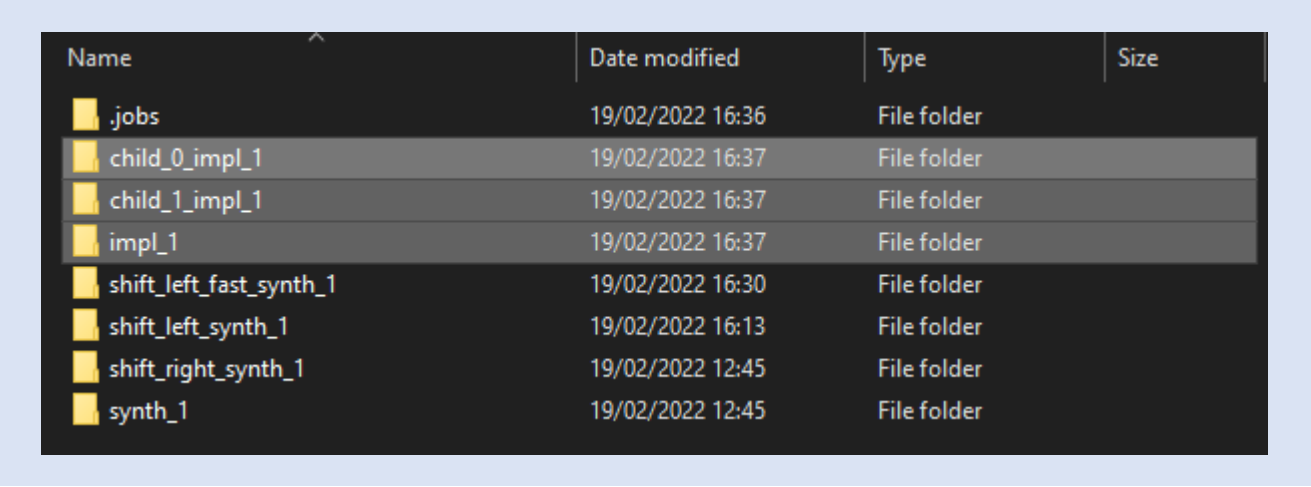
Lab: DFX

Step 25 – Implement the design and generate the bitstreams



Lab: DFX

Step 26 – The implementation directory will show one implementation for the total design and another for each child created. Under these you will find the complete and the partial bitstreams. Both can be programed via Hardware Manager into the target board.



Lab: DFX

Step 27 – Note if targeting a UltraScale device not UltraScale+ the clean.bit must be loaded in first before the partial bitstream.