[Public]

Selecting the Correct Cost Optimized Portfolio Device for your Application

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3. Introduction

One of the most critical steps when designing with programmable logic devices is selecting the most appropriate device for the application. Within the AMD cost optimized portfolio, there are a range of FPGAs and heterogeneous SoCs from which the developer can choose.

The Cost-Optimized Portfolio (COP) includes the AMD 7 series and UltraScale+™ range of devices, all the AMD Spartan™ 7 and AMD Artix™ 7 families, and the AMD Zynq™ 7000 devices below Z7020. In the UltraScale+ family, COP includes the AMD Artix UltraScale+ range and AMD Zynq UltraScale+ devices up to and including the ZU3T.

4. What is the COP and what benefits does it provide developers

These devices are often used across a range of applications, including robotics, medical, industrial, audio, visual, gaming systems, drones, home automation, and networking. For the developer, COP offers significant benefits, including the following:

- System Integration – Several diverse functions can be implemented within the one device, especially when a heterogeneous SoC is used. Integrating several functions within a single device reduces the bill of materials cost and physical size of the product.

- Time to Market – An integrated solution has a faster development time and the flexibility of the FPGA compared to the ASIC-based solutions is significant. AMD also provides a range of development boards and IP for the developer to accelerate application development. Development boards include the AMD Kria™ KV260 and KR260 starter kits, Avnet Ultra96-V2and ZUBoard 1CG. AMD forums, developer programs, and community resources such as the MicroZed Chronicles are also great resources.

- In-Field Update – As product roadmaps and standards evolve, FPGAs and heterogeneous SoCs can be updated in the field. This can also remove the need for recalls, if required.

- Low Risk Solution – Integrated solutions make the design of the circuit board simpler. An integrated solution also helps to reduce the risks associated with Electro Magnetic Interference / Compatibility (EMI/EMC).

- Architectural Flexibility – Both heterogeneous SoC and FPGA devices provide the developer with the ability to architect the solution between sequential processing and parallel processing, using either hard cores within the SoC or a soft processor implemented within the FPGA fabric. Programmable logic also provides any-to-any interfacing capabilities. The unique architecture of heterogeneous SoC devices enable the developer to increase system performance further by creating custom accelerators within the programmable logic, like offloading C algorithms using AMD Vivado™ High-Level Synthesis (HLS).

Devices in the 7 series families will be available through at least 2035 to support the long production runs required for many COP applications such as medical, industrial, and automotive.

A wide diverse range of devices is contained within the COP and these devices provide a range of architectural features which the developer can leverage.

Both FPGA and SoC devices can be split between devices in the 7 series families and those in the UltraScale+ families.

COP devices in the 7 series include the AMD Spartan 7 and Artix 7 families. AMD Spartan 7 devices provide developers with the lowest cost, smallest packaging, and the highest ratio of I/O to logic. If multigigabit transceivers are required, the AMD Artix 7 provides developers with transceivers capable of operating at up to 6.6 Gb/s.

If embedded processing is required within the 7 series range, AMD Zynq 7000 devices from the Z7007S to the Z7020 provide developers with single or dual-core Arm® Cortex®-A9 processors and programmable logic. The UltraScale+ MPSoC families provide developers with either dual or quad A53 processors.

Within the UltraScale+ range, the COP includes the AMD Artix UltraScale+ devices with transceivers capable of supporting line rates at up to 16 Gb/s along with the UltraScale+ MPSoC family in the ZU1 to ZU3T devices.

In addition to the programmable logic and the embedded processor cores, 7 series and UltraScale+ devices within the COP range include these architectural features:

- System Monitor / XADC – An embedded ADC which is capable of monitoring internal voltage rails and temperature which makes it ideal for system safety and security implementation.

- PCIe – PCIe Gen 3 or Gen 4 Endpoint and Root Port implementations with support for several lanes enables high bandwidth data to be transferred on and off chip.

- Integrated Memory – Support for BlockRAM and UltraRAM. BlockRAM are dedicated 36Kb memory blocks that are extremely flexible. Each BlockRAM provides two read and write ports and can be implemented as either a 36 Kb memory or two 18 Kb memories UltraRAM is intended to allow the replacement of off-board memories enabling better overall performance with up to 14 Mb of UltraRAM memory.

- Flexible I/O – I/O support for a range of interfacing from high-speed differential signalling made possible by High Performance I/O (HPIO) to High Density and High Range I/O (HDIO, HRIO) which support 3v3 standards enabling easier integration with commonly used devices.

- Security Features – Multiple levels of security features from bitstream encryption using AES to secure boot utilizing AES, RSA, and SHA. Key management and rolling capabilities are also included on some devices in the COP.

5. Selecting the most appropriate COP device

It can be a daunting task to select between the COP devices so we can use the flow chart below as a guide to help with selection of the most appropriate device for your application.

The first determining factor is if an embedded processor is desired. Depending on the answer to this question, we are either deciding between AMD Zynq 7000 and AMD Zynq UltraScale+ devices or AMD Spartan 7, AMD Artix 7 and AMD Artix UltraScale+ devices.

If an embedded processor is desired, we then need to determine if PL transceivers are desired in the logic design. All AMD Zynq 7000 MPSoC devices have PS GTR high-speed transceivers to implement USB3.0, SATA, and DisplayPort, etc. If transceivers are desired, the AMD Zynq UltraScale+ ZU3T is the appropriate device to be selected because it provides the PL transceivers.

If PL transceivers are not desired, further decision points need to be evaluated depending on the size of the logic resources desired. If less than 80k LUTs are desired, the AMD Zynq 7000 range of devices should be considered. If the desired logic resources exceed more than 80k, the AMD Zynq UltraScale+ MPSoC should be considered. It is worth remembering that when sizing logic resources throughout a project lifecycle, there is often scope and requirement changes that increase the logic resources. Therefore, it's a good idea to size the device to be approximately 60% full when initial size estimates are completed. This enables room for design growth, while also lowering the risk of implementation timing closure issues as the size increases.

One final consideration may be the end application. Many edge applications require a compact form factor to comply with the size, weight, and power requirements. As the programmable logic device is at the heart of the system, size constrained applications can benefit from smaller footprint devices. Thankfully, AMD Zynq UltraScale+ and AMD Artix UltraScale+ devices are available in Integrated FanOut (InFO) packaging and provides a solution which reduces the component board area and the height when compared to flip chip solutions. If you are not familiar with InFO packaging, it enables the removal of the substrate, allowing for the reduced board area and height. Packaging of the selected device may also play an important part in the selection criteria.

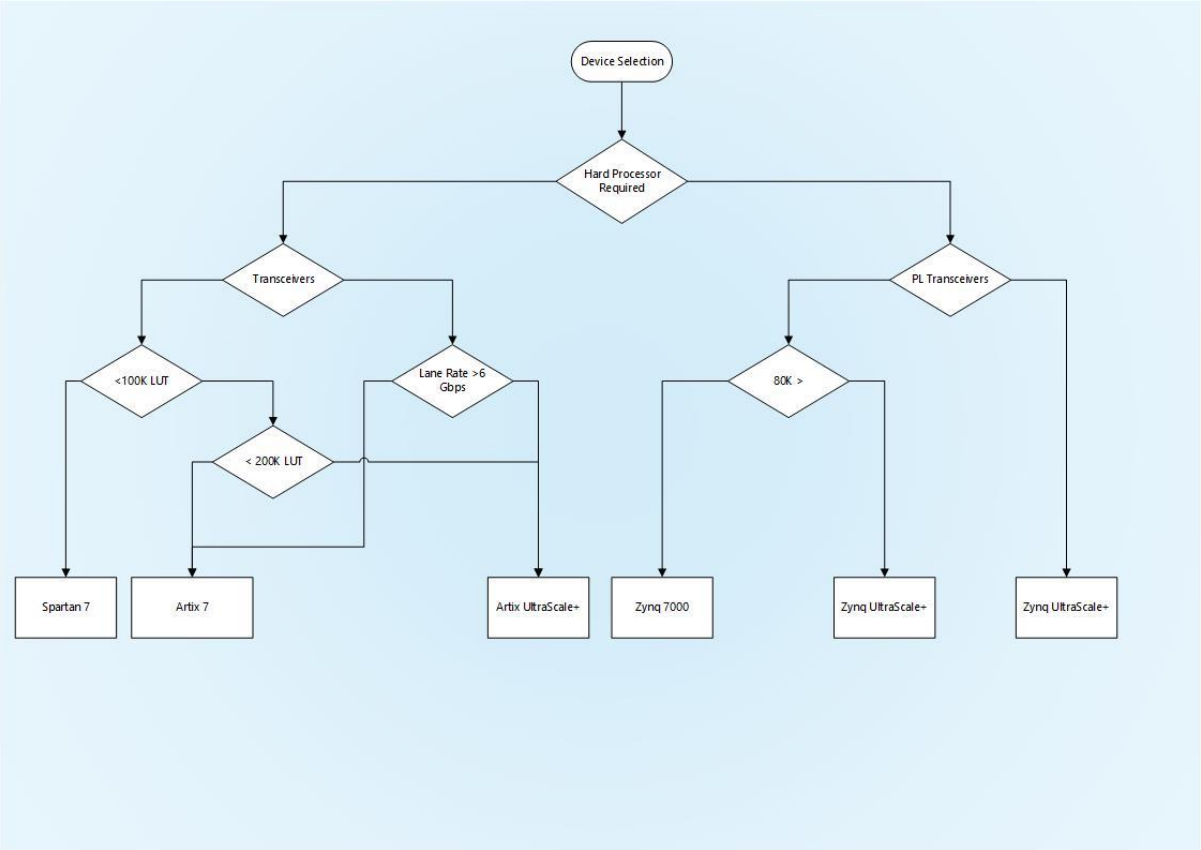

Figure 1 – COP device Selection Flow Chart

If embedded processing is not desired, it must be determined if transceivers are desired. If desired, either the AMD Artix 7 or Artix UltraScale+ families can be considered. If transceivers are not desired, the decision point then becomes one of price, logic resources, and I/O to logic ratio. The developer will typically choose between AMD Spartan 7 devices for lower cost devices or AMD Artix 7 devices for larger logic density. For the larger logic densities, the AMD Artix UltraScale+ range of devices is preferable.

6. Case Studies

Let's look at a couple of simple case studies on device selection. The first example is a frame grabber which is required to capture a scientific image output using a proprietary standard using transceivers. The captured images must be available to download over Ethernet, using the PYNQ framework.

This example needs an embedded processor to communicate with the downstream network and PL transceivers to implement the gigabit transceiver link. The PL will also implement the image capture pipeline and DMA to make the image data available to the processor system. Since PL

transceivers and embedded processors are used for this application, the ZU3T is an appropriate device for consideration.

The second case study example is a SMPTE UH-SDI to PCIe capture card. This card would receive the US-SDI frame, buffer it and make it available over PCIe for onwards processing. This requires high-speed transceivers on the input and output to achieve the high data rates required both for HD-SDI of 12 Gb/s and support for PCIe Gen3 x4 which can support 1GB/s per lane. The deciding factor in this example is the transceiver speeds. The AMD Artix UltraScale+ are the only devices in the COP range which support the 16 Gb/s transceivers.

A final case study would be medical test equipment which is used to analyze and test the waveforms generated by defibrillators. This test equipment would use ADCs to capture the generated waveforms from the defibrillator and the FPGA will capture the waveform into a small external SRAM memory. Once the waveforms have been captured and buffered, the data is then post processed and analyzed to ensure the waveforms are as expected. For this application, no transceivers are required and the estimation of logic sizing is < 100k LUTs with margin. The main driving factor in this is receiving and buffering data in parallel. Since no embedded processor is required and transceivers are not necessary, the logic resource indication of < 100k LUTs of a AMD Spartan 7 FPGA is the correct starting point for the developer to consider.

7. Summary

The variety of granular devices provided within the COP means there is a device to meet the needs of most applications. From the smallest packages in the AMD Spartan 7 FPGA offerings, to compact logic resources with 16 Gb/s transceivers in AMD Artix UltraScale+ devices a high-performance power optimized device and the provision of heterogeneous SoCs with transceivers in the AMD ZU3T, the Cost-Optimized Portfolio provides developers with a range of devices which can be deployed across several applications.

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